# Service Manual

Tektronix

# Tektronix Logic Analyzer Module (TLA7AAx & TLA7ABx)

## 071-1043-00

This document applies to TLA application software version 4.2 and above.

**Warning**
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

**www.tektronix.com**

Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

## WARRANTY

Tektronix warrants that the products that it manufactures and sells will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If a product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; c) to repair any damage or malfunction caused by the use of non-Tektronix supplies; or d) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

**THIS WARRANTY IS GIVEN BY TEKTRONIX IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED. TEKTRONIX AND ITS VENDORS DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. TEKTRONIX' RESPONSIBILITY TO REPAIR OR REPLACE DEFECTIVE PRODUCTS IS THE SOLE AND EXCLUSIVE REMEDY PROVIDED TO THE CUSTOMER FOR BREACH OF THIS WARRANTY. TEKTRONIX AND ITS VENDORS WILL NOT BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES IRRESPECTIVE OF WHETHER TEKTRONIX OR THE VENDOR HAS ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.**

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# General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

*Only qualified personnel should perform service procedures.*

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

### To Avoid Fire or Personal Injury

**Use Proper Power Cord.** Use only the power cord specified for this product and certified for the country of use.

**Use Proper Voltage Setting.** Before applying power, ensure that the line selector is in the proper position for the power source being used.

**Ground the Product.** The TLACAL2 test fixture is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the fixture, ensure that the fixture is properly grounded.

**Ground the Product.** The logic analyzer modules are indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the modules, ensure that the modules are properly grounded indirectly.

**Observe All Terminal Ratings.** To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

**Replace Batteries Properly.** Replace batteries only with the proper type and rating specified.

**Do Not Operate Without Covers.** Do not operate this product with covers or panels removed.

**Use Proper Fuse.** Use only the fuse type and rating specified for this product.

**Avoid Exposed Circuitry.** Do not touch exposed connections and components when power is present.

**Do Not Operate With Suspected Failures.** If you suspect there is damage to this product, have it inspected by qualified service personnel.

**Do Not Operate in Wet/Damp Conditions.**

**Do Not Operate in an Explosive Atmosphere.**

**Keep Product Surfaces Clean and Dry.**

**Provide Proper Ventilation.** Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

## Symbols and Terms

**Terms in this Manual.** These terms may appear in this manual:

***WARNING.*** *Warning statements identify conditions or practices that could result in injury or loss of life.*

***CAUTION.*** *Caution statements identify conditions or practices that could result in damage to this product or other property.*

**Terms on the Product.** These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

**Symbols on the Product.** The following symbol may appear on the product:

# Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

**Do Not Service Alone.** Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

**Disconnect Power.** To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

**Use Care When Servicing With Power On.** Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

# Preface

This is the service manual for the TLA7Axx Series Logic Analyzer Module. Read this preface to learn how this manual is structured, what conventions it uses, and where you can find other information related to servicing this product. Read the Introduction, which follows this preface, for important background information needed before using this manual for servicing this product.

## Manual Structure

A brief description of each chapter of this service manual follows:

- *Specifications* contains a product description of the logic analyzer module and tables of the characteristics and descriptions that apply to it.
- *Operating Information* includes basic installation and operating instructions at the level needed to safely operate and service the logic analyzer module. For complete installation and configuration procedures, refer to the *Tektronix Logic Analyzer Family User Manual*.
- *Theory of Operation* contains circuit descriptions that support general service to the circuit board level.
- *Performance Verification* contains the performance verification procedures for the logic analyzer module, logic analyzer module probes, and the adjustment/verification fixture.
- *Adjustment Procedures* contains the adjustment procedures for the logic analyzer module and the adjustment/verification fixture.
- *Maintenance* contains information and procedures for doing preventive and corrective maintenance on the logic analyzer module. Included are instructions for cleaning, for removal and installation of replacement parts, and for troubleshooting to the circuit board level.
- *Options* contains information on servicing any of the factory-installed options that may be available for the logic analyzer module.
- *Diagrams* contains block diagrams and interconnection diagrams that are useful when isolating failed circuit boards.
- *Mechanical Parts List* includes a table of all replaceable parts, their descriptions, and their Tektronix part numbers.

## Manual Conventions

This manual uses certain conventions that you should be familiar with before attempting service.

**Acquisition Board** The acquisition board is one of the circuit boards inside the logic analyzer module. The circuit board receives and stores acquisition data from the probes and works with the local processor unit (LPU) board to provide logic analysis information to the operator of the logic analyzer.

**Adjustment Procedures** Adjustment procedures check for, and if necessary, correct any adjustment errors discovered when performing functional or performance verification procedures.

**Adjustment/Verification Fixture** The adjustment/verification fixture is a test fixture used to perform the adjustment, functional check, and performance verification procedures. This fixture is also known as the TLACAL2 fixture in this document. Specifications and replaceable parts information are documented in this service manual.

**Certification Procedures** Certification procedures certify a product and provide a traceability path to national standards.

**Functional Verification Procedures** Functional verification procedures verify the basic functionality of the instrument. These procedures include power-on and extended diagnostics, self calibration, as well as semi-automated or manual check procedures. These procedures can be used as incoming inspection purposes. This manual provides information on power-on and extended diagnostics and the self calibration.

**LPU Board** The LPU board is one of the circuit boards inside the logic analyzer module that provides the main communications interface with the acquisition board and the mainframe.

**Maintenance Procedures** Maintenance procedures are used for fault isolation and repair to the circuit board level or to the replaceable part level.

**Modules** Throughout this manual, the term “module” refers to a logic analyzer or digital oscilloscope, or pattern generator unit that mounts inside a mainframe. A module is composed of circuit boards, interconnecting cables, and a user-accessible front panel.

**P6810 General Purpose Logic Analyzer Probe**

This is a 34-channel general purpose probe used with the TLA7Axx series logic analyzers. It provides support for single-ended, differential clocks, and data with no trade-off in channels. It connects to a wide variety of probing accessories including SMT KlipChips for quick connections to a variety of IC pins and connectors.

**P6880 Differential Probe**

This is a 34-channel differential probe used with the TLA7Axx series logic analyzers. This probe is designed for use with differential clocks and single-ended data. It uses a connector-less interface that use a compression contact which is mechanically reliable and minimizes impact on board layout and design. Adaptors are available to connect to Mictor probing interfaces.

**P6860 High Density Probe**

This is a 34-channel high-density probe used with the TLA7Axx series logic analyzers. This probe is designed for use with differential clocks and data with no trade-offs in channels. It uses a connector-less interface that use a compression contact which is mechanically reliable and minimizes impact on board layout and design. Adaptors are available to connect to Mictor probing interfaces.

**Performance Verification Procedures**

Performance verification procedures confirm that a product meets or exceeds the performance requirements for each of the published specifications.

**Replaceable Parts**

This manual refers to any field-replaceable assembly or mechanical part specifically by its name or generically as a replaceable part. In general, a replaceable part is any circuit board or assembly that is listed in the replaceable parts list near the end of this manual.

**Safety**

Symbols and terms related to safety appear in the *Safety Summary* found at the beginning of this manual.

**TLACAL2 Performance Verification and Adjustment Fixture**

This is a test fixture used with the performance verification procedures, adjustment procedures, and certification procedures described in this document. It is used with software to adjust, verify, and certify the P68xx probes and the TLA7Axx series logic analyzers.

## Related Manuals

The following manuals are available as part of the TLA700 Series Logic Analyzer documentation set.

| Manual name | Description | Service use |
|---|---|---|
| Tektronix Logic Analyzer Family User Manual | Provides operating information on the TLA Series Logic Analyzer | Augments operating information found in chapter 2 of this manual |
| TLA715 Portable Mainframe Service Manual | Provides service information for the portable mainframes | Isolating and correcting failures in the portable mainframe |
| TLA721 Benchtop Mainframe and TLA7XM Expansion Mainframe Service Manual | Provides service information for the benchtop mainframe and expansion mainframe | Isolating and correcting failures in the benchtop mainframe, controller, or expansion mainframe |
| TLA7Dx/TLA7Ex Digitizing Oscilloscope Service Manual | Provides service information for the digitizing oscilloscope modules | Isolating and correcting failures in the DSO module. Provides adjustment procedures, performance verification procedures, and certification procedures for the DSO modules |
| TLA7Nx, TLA7Px, & TLA7Qx Logic Analyzer Module Service Manual | Provides service information for the TLA7Nx, TLA7Px, and TLA7Qx logic analyzer modules | Isolating and correcting failures in the logic analyzer module. Provides adjustment procedures, performance verification procedures, and certification procedures for the logic analyzer modules and logic analyzer probes |
| TLA7Lx, & TLA7Mx Logic Analyzer Module Service Manual | Provides service information for the TLA7Lx, and TLA7Mx logic analyzer modules | Isolating and correcting failures in the logic analyzer module. Provides adjustment procedures, performance verification procedures, and certification procedures for the logic analyzer modules and logic analyzer probes |
| TLA7PG2 Pattern Generator Service Manual | Provides service information for the TLA7PG2 pattern generator modules | Isolating and correcting failures in the pattern generator module. Provides adjustment procedures and performance verification procedures for the pattern generator modules and probes |

# Contacting Tektronix

| | |
|---|---|
| **Phone** | 1-800-833-9200* |
| **Address** | Tektronix, Inc.<br>Department or name (if known)<br>14200 SW Karl Braun Drive<br>P.O. Box 500<br>Beaverton, OR 97077<br>USA |
| **Web site** | www.tektronix.com |
| **Sales support** | 1-800-833-9200, select option 1* |
| **Service support** | 1-800-833-9200, select option 2* |
| **Technical support** | Email: techsupport@tektronix.com<br>1-800-833-9200, select option 3*<br>6:00 a.m. – 5:00 p.m. Pacific time |

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
**Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.**

# Introduction

This manual contains information needed to properly service the logic analyzer module, as well as general information critical to safe servicing.

To prevent personal injury or damage consider the following requirements before attempting service:

- The procedures in this manual should be performed only by qualified service personnel.
- Read the *General Safety Summary* and *Service Safety Summary* found at the beginning of this manual.

When using this manual for servicing follow all warnings and cautions.

## Adjustment and Certification Interval

Generally, you should perform the adjustments and certification (calibration) described in the *Performance Verification* and *Adjustment Procedures* chapters in this manual once per year, or following repairs that affect adjustment or calibration.

## Strategy for Servicing

This manual contains information for corrective maintenance of this product:

- Supports isolation of faults to the failed circuit board or assembly level shown in the replaceable parts list
- Supports removal and replacement of those boards or assemblies
- Supports removal and replacement of fuses, knobs, chassis, and other mechanical parts listed in the replaceable parts list

This manual does not support component-level fault isolation and replacement.

## Service Offerings

Tektronix provides service to cover repair under warranty as well as other services that are designed to meet your specific service needs.

Whether providing warranty repair service or any of the other services listed below, Tektronix service technicians are well equipped to service the logic analyzer module.

### Warranty Repair Service

Tektronix warrants this product for one year from date of purchase. (The warranty appears behind the title page in this manual.) Tektronix technicians provide warranty service at most Tektronix service locations worldwide. The Tektronix product catalog lists all service locations worldwide or you can visit us on our web site at http://www.tektronix.com/Measurement/Service. See our latest service offerings and contact us by email.

### Calibration and Repair Service

In addition to warranty repair, Tektronix Service offers calibration and other services that provide cost-effective solutions to your service needs and quality-standards compliance requirements. Our instruments are supported worldwide by the leading-edge design, manufacturing, and service resources of Tektronix to provide the best possible service.

The following services can be tailored to fit your requirements for calibration and/or repair of the logic analyzer module.

### Service Options

Tektronix Service Options can be selected at the time you purchase your instrument. You select these options to provide the services that best meet your service needs.

### Service Agreements

If service options are not added to the instrument purchase, then service agreements are available on an annual basis to provide calibration services or post-warranty repair coverage for the logic analyzer module. Service agreements may be customized to meet special turn-around time and/or on-site requirements.

### Service On Demand

Tektronix also offers calibration and repair services on a “per-incident” basis that is available with standard prices for many products.

### Self Service

Tektronix supports repair to the replaceable-part level by providing for circuit board exchange. Use this service to reduce down-time for repair by exchanging circuit boards for remanufactured ones. Tektronix ships updated and tested exchange boards. Each board comes with a 90-day service warranty.

When you exchange circuit boards, you must supply the following information to allow the board to be preconfigured to the proper PowerFlex level. You can also return the repaired module to your local service center for configuration.

- Model number and serial number
- PowerFlex option upgrade number
- Firmware level

## For More Information

Contact your local Tektronix service center or sales engineer for more information on any of the Calibration and Repair Services just described.

# Specifications

This chapter provides a general description of the TLA7Axx series logic analyzer modules and the TLACAL2 Performance Verification and Adjustment test fixture. This chapter also includes a list of specifications for the logic analyzer module and for the test fixture under *Characteristic Tables* beginning on page 1–2.

## Logic Analyzer Module Description

The TLA7Axx series logic analyzer modules are designed as part of the Tektronix Logic Analyzer Family for use in the TLA700 series logic analyzer mainframes. The logic analyzer module is used as a test and measurement tool for high-speed digital timing and state acquisition across several channels with deep acquisition memory.

Some of the key features of the logic analyzer modules include the following:

- Up to 128 data channels and 8 stored clock or qualifier channels per module
- Ability to merge five modules to provide up to 680 data channels with full clocking and triggering capabilities across all modules
- Software configurable channels, memory depth, and user synchronous speed (PowerFlex)
- Data correlation with other Tektronix logic analyzer modules in a TLA mainframe
- Enhanced clocking to minimize skew between the data bus and the system clock
- Four analog output connectors that send the analog signal of any channel to an oscilloscope or other modules without requiring additional probe connections

The logic analyzer acquires data from the target systems through the P6800 series logic analyzer probes. The following probes are supported:

- P6810 General Purpose Logic Analyzer Probes with flying lead sets. These probes are designed for most general purpose logic analyzer applications.
- P6860 High-Density Logic Analyzer Probes. These probes feature a connectorless system that connect directly to the target system; no adaptors or connectors are required.

- P6880 High Density Differential Logic Analyzer Probes. These probes also feature a connectorless system for differential signals.

Refer to the *P6810, P6860, P6880 Logic Analyzer Probe Instruction Manual* for complete information on the P6800 series logic analyzer probes. This document also contains circuit board design information required for designing the probe interfaces for the target system.

## TLACAL2 Performance Verification and Adjustment Test Fixture Description

The TLACAL2 Performance Verification and Adjustment test fixture is designed to be used with the TLA7Axx series logic analyzer modules and probes for performance verification procedures, certification procedures, and adjustment procedures. These procedures are documented in the *Performance Verification* and *Adjustment Procedures* chapters of this manual.

## Characteristic Tables

All specifications listed in this section are guaranteed unless noted *Typical*. Specification that are marked with the ✓ symbol are checked either directly or indirectly in the *Performance Verification* chapter of this manual. The specifications apply to all variations of the TLA7Axx series logic analyzer module unless otherwise noted.

This section also includes specifications for the performance verification test fixture.

The performance limits under these specifications are valid under the following conditions:

- The logic analyzer modules must have been calibrated (adjusted) at an ambient temperature between +20 °C and +30 °C.
- The logic analyzer modules must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The logic analyzer must have had a warm-up period of at least 30 minutes.

**Table 1-1: Input parameters (with probes)**

| Characteristic | Description |
|---|---|
| ✓ Threshold accuracy (Certifiable parameter) | ± (35 mV + 1% of the threshold voltage setting) |
| Threshold range and step size | Setable from +4.5 V to -2.0 V in 5 mV steps |
| Threshold channel selection | 16 threshold groups assigned to channels. Each probe has four threshold settings, one for each of the clock/qualifier channels and one per group of 16 data channels. |
| ✓ Channel to channel skew | ≤ 400 ps |
| Channel to channel skew (*Typical*) | ≤ 300 ps |
| Sample uncertainty | |
| Asynchronous | Sample period |
| Synchronous | 125 ps |
| Minimum slew rate (*Typical*) | 0.2 V/ns |
| Input voltage range | -2.5 V to +5 V |
| Maximum operating voltage swing | 6.0 V peak-to-peak |
| Probe overdrive | |
| Single ended probes | ± 150 mV or ± 25% of signal swing minimum required beyond threshold, whichever one is greater |
| Differential probes | $V_{pos}$-$V_{neg}$ is ≥ 150m$V_{p-p}$ |
| Maximum nondestructive input signal to probe | ± 15 V |
| Minimum input pulse width (single channel) (*Typical*) | |
| P6860 and P6880 probes | 500 ps |
| P6810 probes | 750 ps |
| Delay time from probe tip to input probe connector (*Typical*) | For P6880 High Density Probe: 7.7 ns ± 60 ps |

**Table 1-2: Analog output**

| Characteristic | Description |
|---|---|
| Number of outputs | Four analog outputs regardless of the module channel width. Any four of the module's channels can be mapped to the four Analog outputs. |
| Attenuation | 10X mode for normal operation<br>5X mode for small signals (-1.5 V to +2.5 V) |
| Bandwidth (*Typical*) | 2 GHz |
| Accuracy (gain and offset) (*Typical*) | ± (50 mV + 2% of signal amplitude) |

**Table 1-3: Channel width and depth**

| Characteristic | Description |
|---|---|
| Number of channels | |
| TLA7AA4, TLA7AB4 | 128 data, 8 clock/qualifier |
| TLA7AA3 | 96 data, 6 clock/qualifier |
| TLA7AA2, TLA7AB2 | 64 data, 4 clock/qualifier |
| TLA7AA1 | 32 data, 2 clock/qualifier |
| Acquisition memory depth | |
| TLA7AAx series | 32 M per channel |
| TLA7ABx series | 64 M per channel |

**Table 1-4: Clocking**

| Characteristic | Description | |
|---|---|---|
| **Asynchronous clocking** | | |
| ✓ Internal sampling period | 500 ps to 50 ms in a 1-2-5 sequence. Storage control can be used to only store data when it has changed (transitional storage)<br>2 ns minimum for all channels<br>1 ns minimum for half channels (using 2:1 Demultiplex mode)<br>0.5 ns minimum for quarter channels (using 4:1 Demultiplex mode) | |
| ✓ Minimum recognizable word[1] (across all channels) | Channel-to-channel skew + sample uncertainty<br>Example for a P6860 high-density probe and a 2 ns sample period:<br>400 ps + 2 ns = 2.4 ns | |
| **Synchronous clocking** | | |
| Master clock channels[2] | Product | Clock channels |
| | 32+2 module | 2 |
| | 64+4 module | 4 |
| | 96+6 module | 4 |
| | 128+8 module | 4 |
| Merged slave clock channels[2]<br>(64+4 channel modules and 32+2 channel modules cannot be merged.) | Product | Clock channels |
| | 96+6 module | 4 |
| | 128+8 module | 4 |

**Table 1-4: Clocking (Cont.)**

| Characteristic | Description | |
|---|---|---|
| Qualifier channels[3] | Product | Qualifier channels |
| | 32+2 module | 0 |
| | 64+4 module | 0 |
| | 96+6 module | 2 |
| | 128+8 module | 4 |
| ✓ Setup and hold window size (data and qualifiers) | P6860 high density probe = 750 ps | |
| Setup and hold window size (data and qualifiers) (*Typical*) | P6860 high density probe = 625 ps | |
| Setup and hold window range | The setup and hold window can be moved for each channel group from +8.0 ns ($T_s$ typical) to -8.0 ns ($T_s$ typical) in 0.125 ns steps (setup time).<br>The setup and hold window can be shifted toward the setup region by 0 ns, 4 ns, or 8 ns. With a 0 ns shift, the range is +8 ns to -8 ns; with a 4 ns shift, the range is +12 ns to -4 ns; with an 8 ns shift, the range is +16 ns to 0 ns. The sample point selection region is the same setup and hold window. Setup times are specified as typical figures. Hold time follows the setup time by the setup and hold window size. | |
| Sample point selection window range | The setup and hold window can be moved for each channel group from +8.0 ns to -8.0 ns in 0.125 ns steps.<br>This window can be shifted toward the positive region by 0 ns, 4 ns, or 8 ns. With a 0 ns shift, the range is +8 ns to -8 ns; with a 4 ns shift, the range is +12 ns to -4 ns; with an 8 ns shift, the range is +16 ns to 0 ns. The sample point selection region is the same setup and hold window. | |
| ✓ Maximum synchronous clock rate | 450 MHz in full-speed mode (2.2 ns minimum between active clock edges)<br>235 MHz in half-speed mode (4.25 ns minimum between active clock edges)<br>120 MHz in quarter-speed mode (8.3 ns minimum between active clock edges)<br>800 MHz on half channels[4]<br>Software controls the selection between full-speed and half-speed modes. | |

**Table 1-4: Clocking (Cont.)**

| Characteristic | Description |
|---|---|
| **Demultiplex clocking (two clock edges required)** | |
| Demultiplex channels (2:1)<br>TLA7AA3, TLA7AA4, TLA7AB4 modules | Any individual channel can be demultiplexed with its partner channel. If multiplexing is enabled, all of the A and D channels are multiplexed; there is no individual selection. Channels demultiplex as follows:<br>A3(7:0) to/from D3(7:0)<br>A2(7:0) to/from D2(7:0)<br>A1(7:0) to/from D1(7:0)<br>A0(7:0) to/from D0(7:0) |
| TLA7AA1, TLA7AA2, TLA7AB2 modules | Any individual channel can be demultiplexed with its partner channel. If multiplexing is enabled, all of the A and D channels are multiplexed; there is no individual selection. Channels demultiplex as follows:<br>A3(7:0) to/from C3(7:0)<br>A2(7:0) to/from C2(7:0)<br>A1(7:0) to/from D1(7:0) 64+4 modules only<br>A0(7:0) to/from D0(7:0) 64+4 modules only |
| Demultiplex channels (4:1)<br>TLA7AA3, TLA7AA4, TLA7AB4 modules | Unlike the 2:1 Demultiplex, the channels within a group of four cannot arbitrarily drive the others.<br>E3(7:0) to E2(7:0), E1(7:0), E0(7:0) 128+8 modules only<br>A3(7:0) to A2(7:0), D3(7:0), D2(7:0)<br>A1(7:0) to A0(7:0), D1(7:0), D0(7:0)<br>C3(7:0) to C2(7:0), C1(7:0), C0(7:0)<br>CK3 to CK2, Q3, Q2 128+8 modules only<br>CK1 to CK0, Q1, Q0 |
| TLA7AA1, TLA7AA2, TLA7AB2 modules | Unlike the 2:1 Demultiplex, the channels within a group of four cannot arbitrarily drive the others.<br>A1(7:0) to A0(7:0), D1(7:0), D0(7:0) 64+4 modules only<br>C3(7:0) to C2(7:0), A3(7:0), A2(7:0) |
| Time between Demultiplex clock edges (*Typical*) | Same limitations as normal synchronous acquisition |
| **Source synchronous clocking** | |
| Clocks per module | Four |
| Clocks with merged modules | When merged, the slave modules have two clocks available from the master module. Including the local clocks, the total is six clocks. |
| Clock groups | Four for a single module and for a merged system |
| Size of clock group valid FIFO | Four stages; this allows four (source synchronous or other) clocks to occur before the clock that completes the Clock Group Valid signal for that group |
| Source synchronous clock alignment window | Channel-to-channel skew only |

**Table 1-4: Clocking (Cont.)**

| Characteristic | Description |
|---|---|
| Source synchronous clock reset | The Clock Group Valid FIFO can be reset in one of the two ways:<br>1. By the overflow of a presettable (1-255) 8-bit counter that counts one of the following clocks: 2 ns Clock or the master "heartbeat" clock (synchronous or asynchronous). An active edge places the reset count to its preset value. An active clock edge will clear the Clock Group Valid reset before the clock gets to the FIFO so that no data is lost.<br>2. By enabling an external reset. In this mode, one of the clock channels must be traded on the master module to act as a level-sensitive reset input. Any one of the clocks can be selected. A polarity selection is available. This mode affects all Clock Group Complete circuits.<br>Neither one of the above modes can be intermixed; one or the other must be selected. |
| **Clocking state machine** | |
| Pipeline delays | Channel groups can be programmed with a pipeline delay of 0 through 7 active clock changes. |

1 **Specification only applies with asynchronous (internal) clocking. With synchronous clocking, the setup and hold window size applies.**

2 **Any or all clock channels can be enabled. For an enabled clock channel, either the rising, falling, or both edges can be selected as active clock edges. Clock channels are stored.**

3 **Qualifier channels are stored.**

4 **This is a special mode and has some limitations such as the clocking state machine and trigger state machine only running at 500 MHz.**

**Table 1-5: TLA7Axx module trigger system**

| Characteristic | Description |
|---|---|
| **Trigger resources** | |
| Word recognizers and range recognizers | 16, word recognizers can be combined to form full width, double bounded range recognizers. The following selections are available:<br>16 word recognizers — 0 range recognizers<br>13 word recognizers — 1 range recognizer<br>10 word recognizers — 2 range recognizers<br>7 word recognizers — 3 range recognizers<br>4 word recognizers — 4 range recognizers |
| Range recognizer channel order | From most-significant probe group to least-significant probe group:<br>C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 Ck1 CK0<br>Missing channels for modules with fewer than 136 channels are omitted. When merged, the range recognition extends across the modules. The master module contains the most-significant groups. |
| Glitch detector (normal asynchronous clock mode) | Channel groups can be enabled to detect glitches.<br>Glitches are subject to pulse width variations of up to $\pm$125 ps |
| Minimum detectable glitch pulse width (*Typical*) | Minimum input pulse width (single channel)<br>P6860 high density probe: 500 ps<br>P6880 differential probe: 500 ps<br>P6810 general purpose probe: 750 ps |
| Setup and hold violation detector (normal asynchronous clock mode) | Any channel group can be enabled to detect a setup or hold violation. The range is from 8.0 ns before the clock edge to 8.0 ns after the clock edge in 0.125 ns steps. The channel setup and hold violation size can be individually programmed.<br>The range can be shifted towards the positive region by 0 ns, 4 ns, or 8 ns. With a 0 ns shift, the range is +8 ns to -8 ns; with a 4 ns shift, the range is +12 ns to -4 ns; with an 8 ns shift, the range is +16 ns to 0 ns. The sample point selection region is the same as the setup and hold window.<br>Any setup value is subject to variation of up to the channel skew specification. Any hold value is subject to variation of up to the channel skew specification. |
| Transition detector | 16 transition detectors.<br>Any channel group can be enabled or disabled to detect a rising transition, a falling transition, or both rising and falling transitions between the current valid data sample and the previous valid data sample. |
| Counter/timers | 2 counter/timers, 51 bits wide, can be clocked up to 500 MHz<br>Maximum count is $2^{51}$<br>Maximum time is $4.5 \times 10^6$ seconds or 52 days<br>Counters can be used as setable, resetable, and testable flags. Counters can be reset, do nothing, incremented, or decremented. Timers can be reset, started, stopped, or not changed. Counters and timers have zero reset latency and one clock terminal count latency. |
| Signal In 1 | A backplane input signal. |

**Table 1-5: TLA7Axx module trigger system (Cont.)**

| Characteristic | Description |
|---|---|
| Signal In 2 | A backplane input signal. |
| Trigger In | A backplane input signal that causes the main acquisition and the MagniVu acquisition to trigger if they are not already triggered. |
| Active trigger resources | 16 maximum (excluding counter/timers)<br>Word recognizers are traded off one-for-one as Signal In 1, Signal In 2, glitch detection, setup and hold detection, or transition detection resources are added. |
| Trigger states | 16 |
| ✓ Trigger state sequence rate | Same rate as valid data samples received. 500 MHz maximum. |
| **Trigger machine actions** | |
| Main acquisition trigger | Triggers the main acquisition memory |
| Main trigger position | Programmable to any data sample (2 ns boundaries) |
| MagniVu trigger | Main acquisition machine controls the triggering of the MagniVu memory |
| MagniVu trigger position | Programmable within 2 ns boundaries and separate from the main acquisition memory trigger position |
| Increment/decrement counter | Counter/timers used as counters can be incremented or decremented. |
| Start/stop timer | Either of the two counter/timers used as timers can be started or stopped. |
| Reset counter/timer | Either of the two counter/timers can be reset.<br>When a counter/timer used as a timer is reset, the timer continues in the started or stopped state that it was prior to the reset. |
| Reloadable word recognizer (snapshot) | Loads the current acquired data sample into the reference value of the word recognizer via a trigger machine action. All data channels are loaded into their respective word recognizer reference register on a one-to-one manner. |
| Reloadable word recognizer latency | 378 ns |
| Signal Out | A signal sent to the backplane to be used by other modules |
| Trigger Out | A signal sent to the backplane to trigger other modules |
| **Storage control** | |
| Storage | Storage is allowed only if a specific condition is met. The condition can use any of the trigger resources except for counter/timers. Storage commands defined in the current trigger state will override the global storage control.<br>Storage can be used to start the acquisition with storage initially turned on (default setting) or off. |
| By event | Storage can be turned on or off; only the current sample can be stored. Event storage control overrides any global storage commands. |
| Block storage (store stretch) | When enabled, 31 samples are stored before and after the valid sample.<br>This allows the storage of a group of samples around a valid data sample when storage control is being used. This only has meaning when storage control is used. Block storage is disallowed when glitch storage or setup and hold violation storage is enabled. |

**Table 1-5: TLA7Axx module trigger system (Cont.)**

| Characteristic | Description |
|---|---|
| Glitch violation storage | Glitch violation information can be stored to acquisition memory with each data sample when asynchronous clocking is used. The acquisition data storage size is reduced by half when this mode is enabled (the other half holds violation information). The fastest asynchronous clock rate is reduced to 4 ns. |
| Setup and hold violation storage | Setup and hold violation information can be stored to acquisition memory with each data sample when synchronous clocking is used. The acquisition data storage size is reduced by half when this mode is enabled (the other half holds violation information). The maximum synchronous clock rate in this mode is 235 MHz. |

**Table 1-6: MagniVu acquisition**

| Characteristic | Description |
|---|---|
| MagniVu sampling period | Data is asynchronously sampled and stored every 125 ps in a separate MagniVu (high-resolution) memory. The storage speed can be changed by software to 250 ps, 500 ps, or 1000 ps with no loss in memory depth so that the high resolution memory covers more time at a higher resolution. |
| MagniVu memory depth | Approximately 16 K per channel. The MagniVu memory is separate from the main acquisition memory. |

**Table 1-7: Merged modules**

| Characteristic | Description |
|---|---|
| Number of merged modules | 2, 3, 4, or 5 adjacent modules can be merged. Only 102-channel modules or 136-channel modules can be merged. Merged modules can have unequal channel widths and channel depths.<br><br>See Figure 1-1 for location of modules in a merged configuration. |
| Number of channels after merging | The sum of all channels available on each of the merged modules including clocks and qualifiers. No channels are lost when modules are merged. |
| Merged system acquisition depth | Channel depth is equal to that of the shallowest module. |
| Number of clock and qualifier channels after merging | The qualifier channels on the slave modules can only be used as data channels. They cannot influence the actual clocking function of the logic analyzer (for example, log strobe generation).<br><br>The clock channels on the slave TLA7Axx modules can capture data on those modules for source-synchronous applications. Each slave module contributes four additional clock channels to the merged set. All clock and qualifier channels are stored to acquisition memory. |
| Merged system trigger resources | The same as a single module except for word recognizer width, setup and hold violation detector width, glitch detector width, and transition detector width has increased to equal that of the merged channel width. Range recognizers will increase to the merged channel width up to three modules; range recognition is not supported on the two outside slave modules. |
| Merged range significance | Most significant Master, Slave 1, Slave 2 |

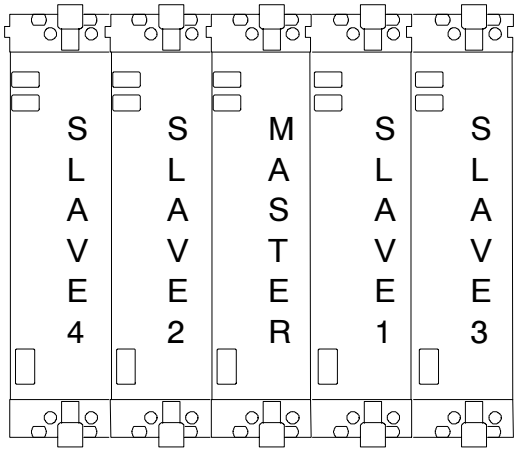


**Figure 1-1: Location of modules in merged configurations**

**Table 1-8: Data handling**

| Characteristic | Description |
|---|---|
| Nonvolatile memory retention time (*Typical*) | The battery life is integral to the NVRAM; battery life is > 10 years. |

**Table 1-9: Environmental**

| Characteristic | Description |
|---|---|
| Temperature | |
| Operating | 5 °C to +40 °C/hour maximum gradient, non-condensing<br>The maximum operating temperature is derated at altitudes above 305 m (1000 ft.) by 1 °C per 305 m (1000 ft.) above 1525 m (5000 ft.) altitude |
| Non-operating | -20 °C to +60 °C with 15 °C/hour maximum gradient, without disk media installed in disk drives. |
| Humidity | |
| Operating | (No media in floppy or CD in mainframe drive):<br>20% to 80% relative humidity, noncondensing, maximum wet-bulb temperature of +29 °C (derates relative humidity to 45% at 40 °C) |
| Non-operating | (No media in floppy or CD in mainframe drive):<br>8% to 80% relative humidity, non-condensing, maximum wet-bulb temperature of +29 °C (derates relative humidity to 22% relative humidity at 50 °C) |
| Altitude | |
| Operating | To 3048 m (10,000 ft.) provide maximum ambient temperature is derated by 1 °C per 305 m (1000 ft.) above 1525m (5000 ft.) |
| Non-operating | 12192 m (40,000 ft.) |

**Table 1-10: Mechanical**

| Characteristic | Description |
|---|---|
| Material | Chassis parts are constructed of aluminum alloy. The front panel is constructed of plastic laminated to steel front panel. Circuit boards are constructed of glass laminate. |
| Weight | |
| 136-channel module | 2.438 kg (5 lb 6 oz.) |
| 102-channel module | 2.381 kg (5 lb 4 oz.) |
| 68-channel module | 2.282 kg (5 lb 0.5 oz.) |
| 34-channel module | 2.254 kg (4 lb 15.5 oz.) |
| Shipping weight | 3.515 kg (7 lb 12 oz.) for 136-channel module when packaged for domestic shipment |
| Overall dimensions | |
| Height | 262 mm (10.32 in) |
| Width | 61 mm (2.39 in) with merge connector in the recessed position<br>Width increases by 10.41 mm (0.41 in) with merge connector in the extended position |
| Length | 373 mm (14.7 in) |
| Mainframe interlock | 1.4 ECL keying is implemented |

**Table 1-11: TLA7Axx Logic Analyzer Module Certifications and compliances**

| Category | Standards or description | |
|---|---|---|
| EC Declaration of Conformity - EMC | Meets intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities: | |
| | EN 61326 | EMC requirements for Class A electrical equipment for measurement, control and laboratory use.[1] |
| | IEC 61000-4-2 | Electrostatic discharge immunity (Performance criterion B) |
| | IEC 61000-4-3 | RF electromagnetic field immunity (Performance criterion A) |
| | IEC 61000-4-4 | Electrical fast transient / burst immunity (Performance criterion B) |
| | IEC 61000-4-5 | Power line surge immunity (Performance criterion B) |
| | IEC 61000-4-6 | Conducted RF immunity (Performance criterion A) |
| | IEC 61000-4-11 | Voltage dips and interruptions immunity (Performance criterion B) |
| | EN 61000-3-2 | AC power line harmonic emissions |

[1] **Emissions which exceed the levels required by this standard may occur when this equipment is connected to a test object.**

**Table 1-12: TLACAL2 Performance verification and adjustment fixture characteristics**

| Characteristic | Description |
|---|---|
| Input channels | One external clock input<br>Input voltage < 1 V referenced to ground, 50 Ω termination |
| P6860 deskew and minimum pulse timing outputs | 34 + 5 grouped into three P6860 connectors, two with 17 channels and one with five channels |
| P6860-setup and hold outputs | 136 grouped into eight 17-channel connectors |
| P6880 deskew and minimum pulse timing outputs | 34 + 5 grouped into three P6860 connectors, two with 17 channels and one with five channels |
| P6860/80 gain and offset outputs | 68 grouped into four 17-channel connectors |
| P6810 gain and offset outputs | 34 grouped into four 8-channel connectors and one 2-channel connector for the clocks |
| Analog output SMB inputs | Four inputs with 50 Ω termination each |
| DMM test points | One connection to a GPIB-controlled digital voltmeter |
| Number of module interface connector (MIC) boards connected at one time | Four. Each board requires a ribbon cable and two MCX cable attachments to the main board |
| Number of Probe interface connector (PIC) boards connected at one time | One. The board must be connected to the ribbon connector labeled PIC. |
| Timing section output amplitude | 100E Motorola ECLinPS family outputs referenced to +2 V amplitude |
| Gain/Offset output voltage range | -5 V to +5 V |
| MIC board test current range | ±3 mA |
| **Interface ports** | |
| RS-232 | 9-pin RS-232 serial communications interface |
| JTAG | Programming interface for the xilinx CPLD |
| **Power distribution system** | |
| Power consumption | 40 W maximum |
| Source voltage and frequency | 100 $V_{RMS}$ to 240 $V_{RMS}$ ±10%, 50 Hz to 60 Hz continuous range CAT II<br>115 $V_{RMS}$ ±10%, 400 Hz, continuous range CAT II |
| Fuse ratings | |
| 100 V to 120 V operation | 5.0 mm x 20 mm, 1.0 A FAST 250 V; Tektronix part number 159-0356-00 |
| 200 V to 240 V operation | 5.0 mm x 20 mm, 0.5 A FAST 250 V; Tektronix part number 159-0351-00 |
| Internal power supply | 5.0 mm x 20 mm, 3.15 A, 250 V |

**Table 1-12: TLACAL2 Performance verification and adjustment fixture characteristics (Cont.)**

| Characteristic | Description |
|---|---|
| Secondary power supply output voltages | |
| +15 V | +10%, -3% |
| -15 V | ±5% |
| +12 V | ±10% |
| +5 V | ±2% |
| +3 V | ±100 mV |
| -3 V | ±100 mV |
| +2 V | ±100 mV |
| Secondary power supply output voltage ripple | |
| ±3 V | < 50 $mV_{P-P}$ with respect to ground |
| +2 V | < 50 $mV_{P-P}$ with respect to ground |
| **Cooling clearance** | 51 mm (2 in) front, sides, and rear. Prevent blockage of airflow to bottom of instrument by placing on a solid, noncompresable surface. |
| **Atmospherics** | |
| Temperature | |
| Operating | 20 °C to 30 °C |
| Non-operating | +5 °C to +50 °C with 15 °C gradient per hour noncondensing |
| Humidity | |
| Operating | 20% to 80% relative humidity, noncondensing |
| Non-operating | 8% to 80% relative humidity, noncondensing and as limited by a maximum wet bulb temperature of +40 °C |
| Altitude | |
| Operating | To 3048 m (10,000 ft.) |
| Non-operating | To 12192 m (40,000 ft.) |
| **Mechanical shock** | 30 Gs maximum |

**Table 1-13: TLACAL2 Performance verification and adjustment fixture certifications and compliances**

| Category | Standards or description | |
|---|---|---|
| EC Declaration of Conformity - Low Voltage | Compliance was demonstrated to the following specification as listed in the Official Journal of the European Communities: | |
| | Low Voltage Directive 73/23/EEC, amended by 93/68/EEC | |
| | EN 61010-1/A2:1995 | Safety requirements for electrical equipment for measurement control and laboratory use. |
| U.S. Nationally Recognized Testing Laboratory Listing | UL3111-1 | Standard for electrical measuring and test equipment. |
| Canadian Certification | CAN/CSA C22.2 No. 1010.1 | Safety requirements for electrical equipment for measurement, control, and laboratory use. |
| Additional Compliance | IEC61010-1/A2:1995 | Safety requirements for electrical equipment for measurement, control, and laboratory use. |
| Installation (Overvoltage) Category Descriptions | Terminals on this product may have different installation (overvoltage) category designations. The installation categories are: | |
| | CAT III | Distribution-level mains (usually permanently connected). Equipment at this level is typically in a fixed industrial location. |
| | CAT II | Local-level mains (wall sockets). Equipment at this level includes appliances, portable tools, and similar products. Equipment is usually cord-connected. |
| | CAT I | Secondary (signal level) or battery operated circuits of electronic equipment. |
| Pollution Degree Descriptions | A measure of the contaminates that could occur in the environment around and within a product. Typically the internal environment inside a product is considered to be the same as the external. Products should be used only in the environment for which they are rated. | |
| | Pollution Degree 1 | No pollution or only dry, nonconductive pollution occurs. Products in this category are generally encapsulated, hermetically sealed, or located in clean rooms. |
| | Pollution Degree 2 | Normally only dry, nonconductive pollution occurs. Occasionally a temporary conductivity that is caused by condensation must be expected. This location is a typical office/home environment. Temporary condensation occurs only when the product is out of service. |
| | Pollution Degree 3 | Conductive pollution, or dry, nonconductive pollution that becomes conductive due to condensation. These are sheltered locations where neither temperature nor humidity is controlled. The area is protected from direct sunshine, rain, or direct wind. |
| | Pollution Degree 4 | Pollution that generates persistent conductivity through conductive dust, rain, or snow. Typical outdoor locations. |
| Equipment Type | Test and measuring | |
| Safety Class | Class 1 (as defined in IEC 61010-1, Annex H) - grounded product | |
| Overvoltage Category | Overvoltage Category II (as defined in IEC 61010-1, Annex J) | |
| Pollution Degree | Pollution Degree 2 (as defined in IEC 61010-1). Note: Rated for indoor use only. | |

# Operating Information

This chapter provides a high-level overview of installation instructions and operating information for the logic analyzer module. The operating information is limited to the functions you need to perform the procedures found in this document. You can find detailed operating instructions in the *Tektronix Logic Analyzer Family User Manual* and in the online help.

## Installation

The *Tektronix Logic Analyzer User Manual* provides detailed installation instructions for the logic analyzer module and the mainframes. This section contains a summary of those installation procedures. This section also describes the installation procedures for the TLACAL2 Performance Verification and Adjustment fixture; this fixture is required for the TLA7Axx series logic analyzer module performance verification procedures, certification procedures, and adjustment procedures.

### Logical Address

Every plug-in module in the logic analyzer must have a unique logical address; no two modules can have the same address. Two rotary switches on rear panel select the logical address (see Figure 2–1 for the switch locations). When servicing the logic analyzer module, you should have no need for changing the address. However, in most cases the switches should be set to FF, the factory default setting to enable dynamic auto configuration.

---

***NOTE***. *Do not set the logic analyzer module logical address to 00. Logical address 00 is reserved for the controller.*

---

**Dynamic Autoconfiguration** With Dynamic Auto Configuration (recommended) selected (hexadecimal FF or decimal 255), the logic analyzer automatically sets the address to an unused value. For example, if there are modules set to addresses 01 and 02 already in your system, the resource manager will automatically assign the logic analyzer module an address other than 01 or 02.

**Static Logical Address** Static logical address selections set the address to a fixed value. A static logical address ensures that the logic analyzer module address remains fixed for compatibility with modules that require a specific address value. Remember that each module within the logic analyzer must have a unique address to avoid communication problems.

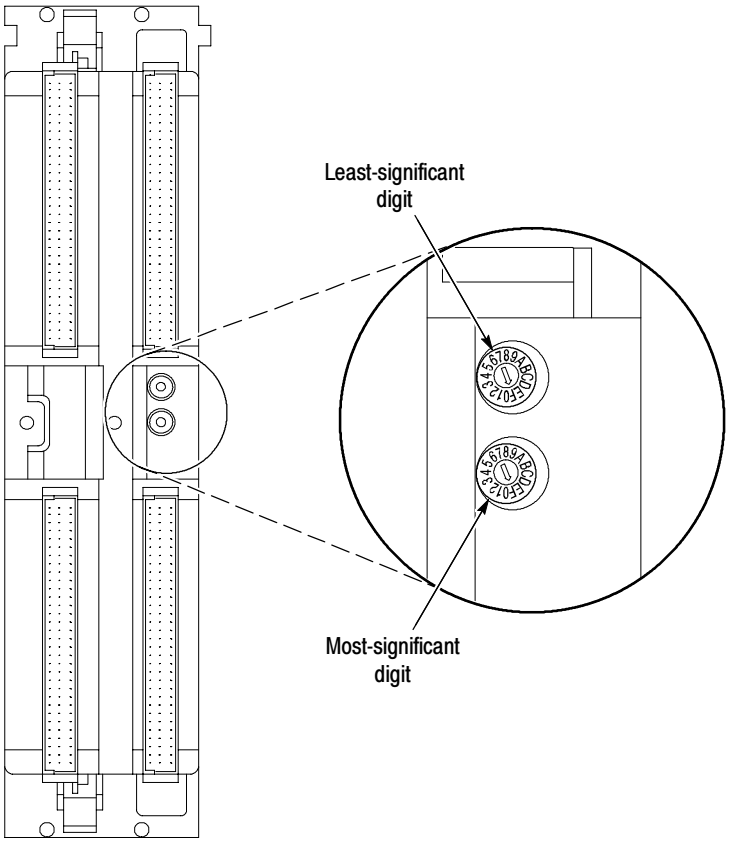


**Figure 2- 1: Logical address switches**

## Merged Modules

You can combine up to five logic analyzer modules to create a single module that operates off a single time base. This process is called merging modules. The procedures for merging modules is described under *Merged Modules* beginning on page 2–14.

## Module Installation

Install the modules in a mainframe before applying power to the mainframe. Before installing the modules, determine if you want to merge the modules. You must physically connect the module together before installing them in the mainframe.

Slide the module all of the way into the mainframe. Use the injector/ejector handles to seat the module and then hold the modules in place by tightening the retaining screws (see Figure 2–2 on page 2–3). If you are installing merged modules, slide them into the mainframe as a group and then seat them in place individually.

For more detailed information on installing modules, refer to *Appendix D: TLA700 Module Installation* in the *Tektronix Logic Analyzer Family User Manual*.

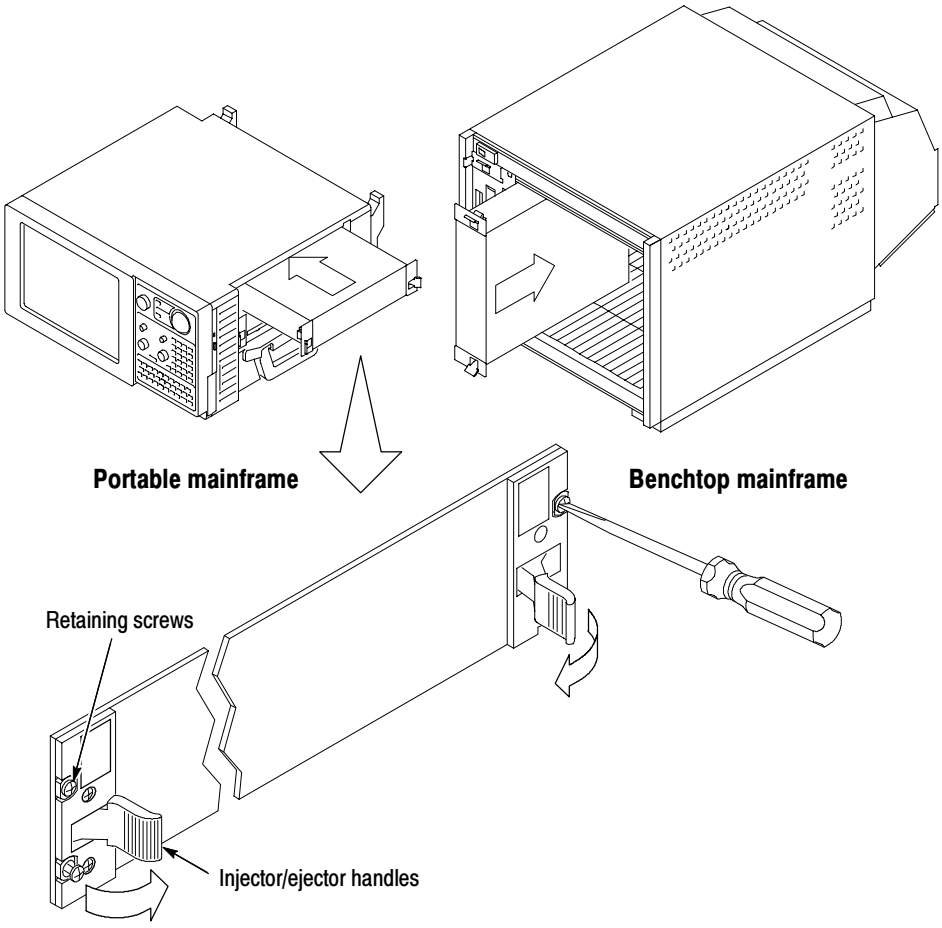


**Figure 2-2: Installing modules in the mainframe**

## TLACAL2 Fixture Installation

The TLACAL2 Performance Verification and Adjustment test fixture is required to perform the performance verification procedures, certification procedures, and adjustment procedures. If you will not be running the performance verification or adjustment procedures, you can skip this section.

You will need to connect the TLACAL2 fixture to the logic analyzer and associated test equipment before running procedures. A complete list of test equipment is listed in Table 4–1 on page 4–3.

***CAUTION.*** *Static discharge can damage the TLACAL2 fixture and its associated circuit boards. Make sure that you install the fixture in a static-free environment. Always wear a grounded wrist strap while handling the TLACAL2 fixture and its associated equipment. For more information on antistatic procedures, see* Preventing Electrostatic Discharge *on page 6–1.*

Due to the short cable lengths, you must decide upon a location for the TLACAL2 fixture that allows you to connect the test fixture to the logic analyzer module under test (less than two feet). The fixture can be placed on top of a benchtop mainframe or on a static free work surface adjacent to the logic analyzer.

The following steps assume that you have all the required test equipment necessary to run the performance verification procedures, certification procedures, and adjustment procedures. See Table 4–1 on page 4–3 for a complete list of test equipment.

1. If you have not already done so, power down the mainframe and install the logic analyzer module.
2. Connect the RS-232 cable from the COM A connector of the logic analyzer mainframe to the RS-232 connector on the performance verification fixture.

***NOTE.*** *When using GPIB, make sure that you select unique GPIB addresses on the individual instruments to avoid conflicts.*

3. Connect the GPIB cable from the digital multimeter to the oscilloscope.
4. Connect the iView cable from the USB connector on the logic analyzer mainframe to the GPIB connector on the DMM.

***NOTE.*** *Steps 5 and 6 assume that you will be connecting the TLACAL2 fixture to a 136-channel logic analyzer module. You only need to connect one MIC board and one ribbon cable per 34 channels on the logic analyzer module. If your logic analyzer module has less than 136 channels, you can reduce clutter by only connecting the cables that you need for your instrument configuration.*

5. Connect one end of the ribbon cables to the MIC 0/PIC, MIC 1, MIC 2 and MIC 3 connectors on the performance verification fixture.

***NOTE**. The MIC boards and the PIC board look very similar. The MIC boards have two coaxial cable connections while the PIC board has only one (see Figure 2–3).*

*To quickly identify the MIC and PIC boards, you may want to attach a small label on the plastic housing of the MIC connector with the name of the MIC and PIC connectors (such as MIC0).*

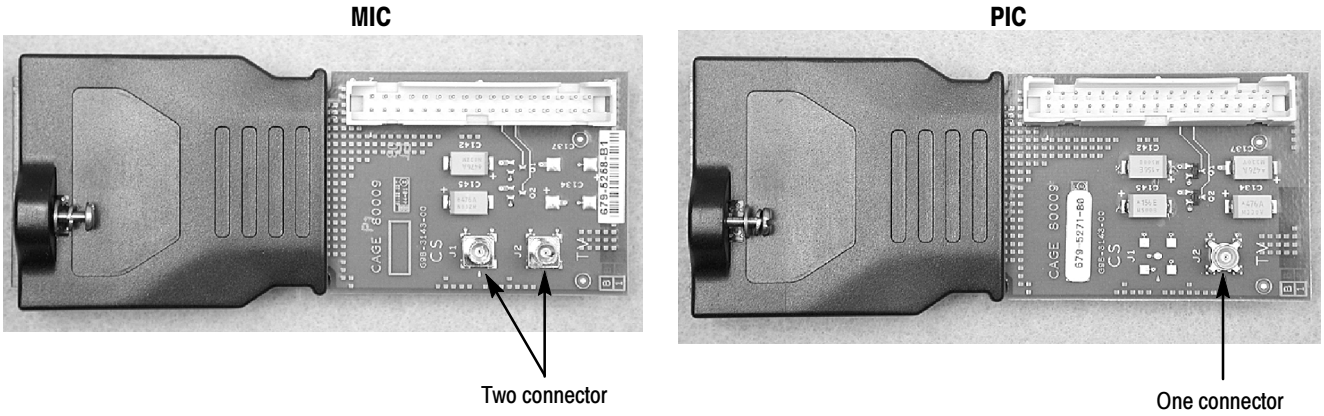


**Figure 2-3: MIC and PIC board identification**

6. Connect the four MIC boards (labeled 6795258B1 on the anti-static bags) to the other end of each ribbon cable.
7. Connect a black coaxial cable from each of the Current Source (CS) connectors from the performance verification fixture to the CS connectors on each of the MIC boards.
8. Attach one of the color bands to each end of the current source cables to help you identify them. Use your own color-scheme when connecting the color bands.
9. Connect a black coaxial cable from each of the Test Voltage (TV) connectors from the performance verification fixture to the TV connectors on each of the MIC boards.

***CAUTION.** Power down the performance verification test fixture, before connecting or disconnecting any Module Interface Cards (MICs) or the Probe Interface Cards (PICs). Connecting or disconnecting items to the performance verification fixture while power is applied will damage the performance verification fixture or other test equipment.*

**10.** Connect the power cord to the performance verification fixture.

**11.** Leave the four P6041 cables and the PIC board disconnected. You will connect these to the performance verification fixture and logic analyzer module during the actual procedures.

Figure 2–4 shows the TLACAL2 fixture with the major components connected to the logic analyzer.

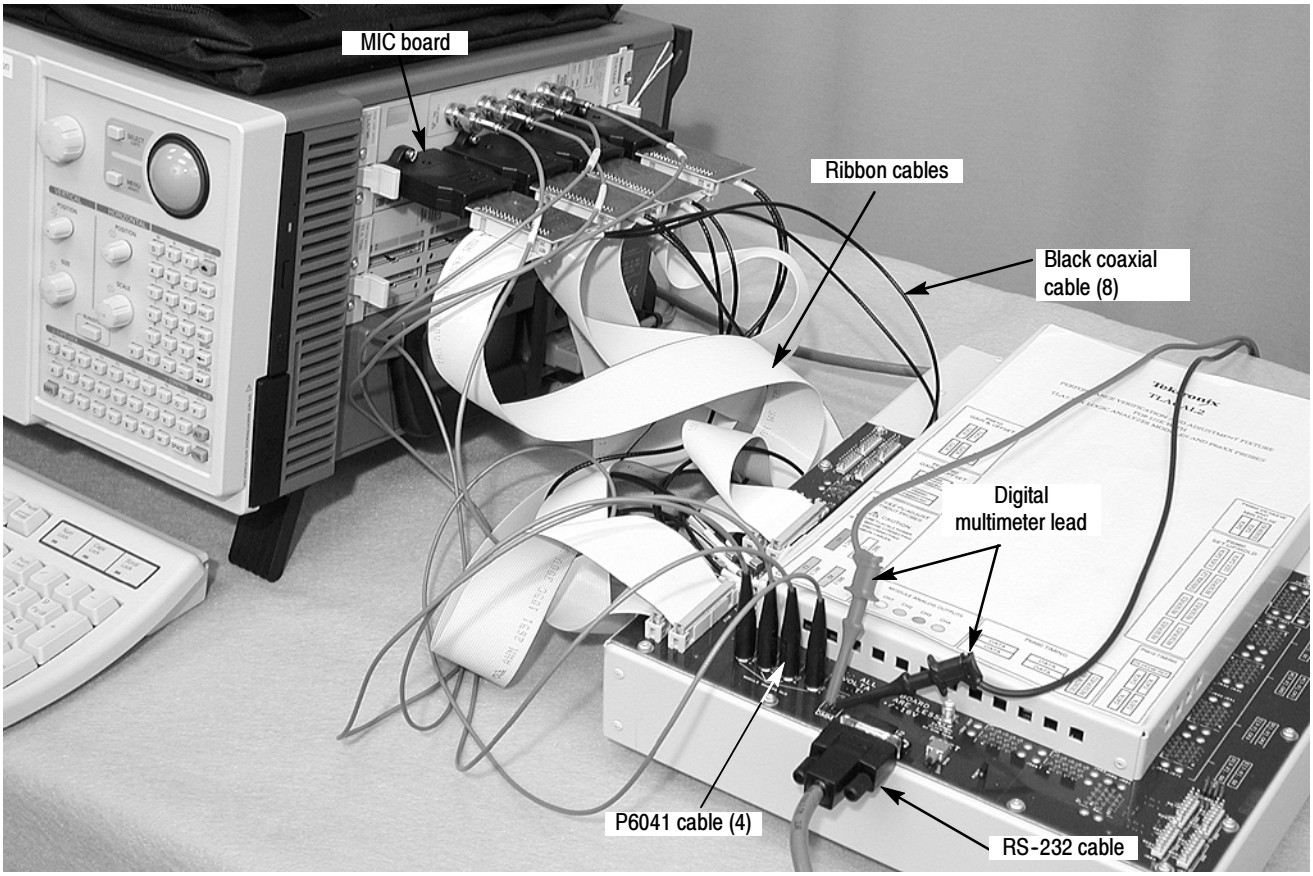


**Figure 2-4: TLACAL2 performance verification and adjustment test fixture**

## Software Installation

The logic analyzer module operation is controlled by the Tektronix logic analyzer application software located on the hard disk of the mainframe. This software is installed when you purchased your logic analyzer or when you upgrade the software through one of the TLA7UP Field Upgrade Kit options. The logic analyzer module contains firmware which may need to be upgraded to function with the latest system software version; the firmware upgrade procedure is provided with the TLA7UP Field Upgrade Kit. The procedure is also described in this manual under *Updating or Restoring the Logic Analyzer Firmware* beginning on page 6–35.

To service the logic analyzer module and to complete the performance verification or adjustment procedures, you must install the Performance Verification software from disc 1 of the TLA application CD on the mainframe's hard disk.

### Verify the Performance Verification Software Version

If your logic analyzer mainframe already has the performance verification software installed on the hard disk, you should verify that the software version matches that of the TLA application software. The TLA application software version is printed on disc 1 of the Tektronix Logic Family Analyzer application software CD.

If the version of the performance verification software on the hard disk does not match the CD label or the TLA application software, you must delete the older version before you can install the newer version. Refer to *Removing the Software* for instructions on removing the software.

### Install the Performance Verification Software

Use the following steps to install the performance verification software:

1. Close all open applications.
2. Insert Disc 1 of the Tektronix Logic Analyzer Family application software CD in the CD-ROM drive.
3. On the desktop select Start → Run to display the Run dialog.
4. In the Run dialog box, enter the following path or use the Browse button to navigate to the path:

   ```
   D:\TLA7Axx PV Adjust\Setup.exe
   ```

5. Click OK to begin the installation program and then follow the on-screen instructions to install the software.
6. Remove the CD when the installation is complete.

### Removing the Software

Use the following steps to remove the performance verification software from the hard disk in the mainframe. These steps are necessary when you want to upgrade the performance verification software.

1. On the desktop, select Start → Settings→ Control Panel
2. Double-click on Add/Remove Programs.
3. Select TLA7AxxPVAdjust.
4. Click the Change/Remove button.

## Operating Information

This section provides a high-level overview of the controls and connectors of the logic analyzer module. It provides a high-level overview of the logic analyzer user interface and software.

### Front Panel

Figure 2–5 shows the connectors and indicators on the front panel of a 136-channel logic analyzer module. Modules with fewer channels look and operate the same, but without the additional probe connectors.

**Injector/Ejector Handles.** The injector/ejector tabs are used to seat and unseat the modules in the mainframe.

**READY Indicator.** The READY indicator lights continuously after the logic analyzer module successfully completes the power-on process. If the indicator fails to light within five seconds of power-on, an internal module failure may be present.

**ACCESSED Indicator.** The ACCESSED indicator lights anytime the controller accesses the logic analyzer module.

**ARM'D Indicator.** The ARM'D indicator lights when the logic analyzer module is armed during an acquisition.

**TRIG'D Indicator.** The TRIG'D indicator lights when the logic analyzer module triggers and stays on until the module finishes acquiring data.

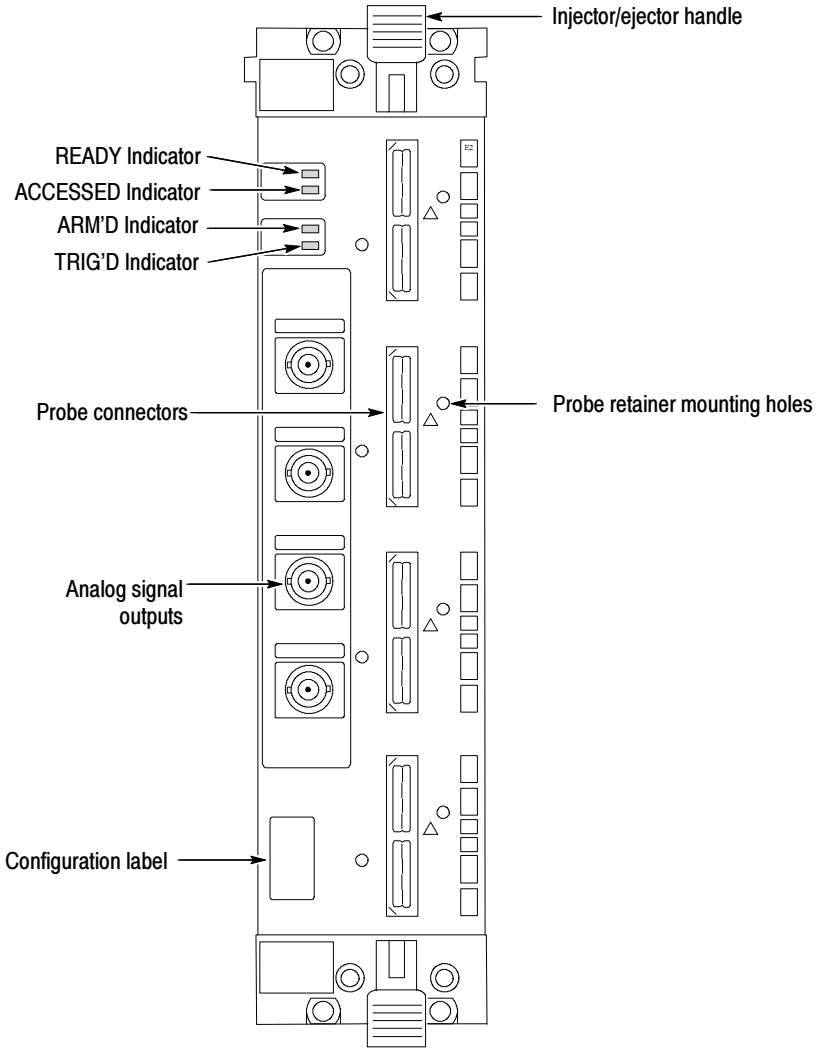


**Figure 2-5: Front panel of the logic analyzer module**

**Probe Connectors.** The probe connectors are color-coded to match the labels on the probes. Each probe connector accepts a 34-channel active probe consisting of 32 data channels and two clock/qualifier channels.

**Probe Retainer Mounting Holes.** The threaded probe retainer mounting holes provide a means of securely holding the probes in place. You must tighten the retaining screws to ensure a good ground connection for the probes to the module.

**Analog Outputs.** Each module has four analog output BNC connectors regardless of the number of acquisition channels. The analog output connectors allow you to tap into the analog signal of any channel and connect the signals to an external instrument, such as an oscilloscope. This feature allows you to view the analog component of a selected channels without requiring a separate oscilloscope probe connection.

**Configuration Label.** The configuration label indicates the speed and memory depth of the logic analyzer module.

## Merge Cable Connectors

Merge connectors on both sides of the module allow you to merge up to five individual modules to create a single module with up to 680 channels with full clock and trigger functionality. The 34-channel and 68-channel modules do not have merge connectors.

The merge connector on the left side of the module can be physically extended to connect with the connector of an adjacent module. The connector is shipped in the recessed position and must be extended when merging modules (see Figure 2–6).

The merge connector on the right side of the module provides play between modules allow easy installation of the module set in a mainframe.

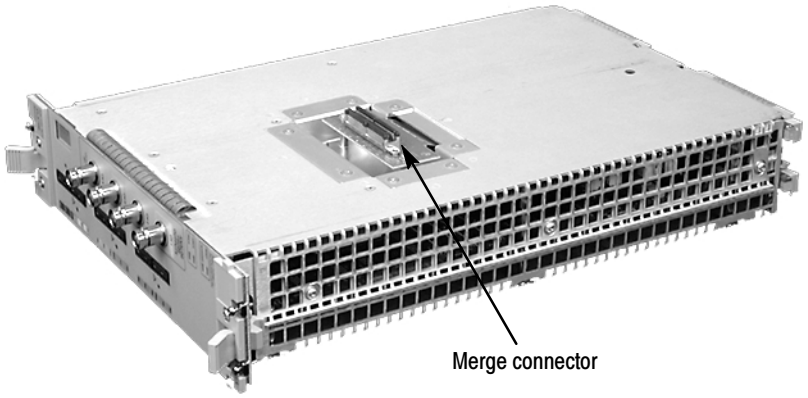


**Figure 2- 6: Merge connector (shown in the extended position)**

## Rear Panel

Figure 2–7 shows the connectors and controls on the rear panel of the logic analyzer module.

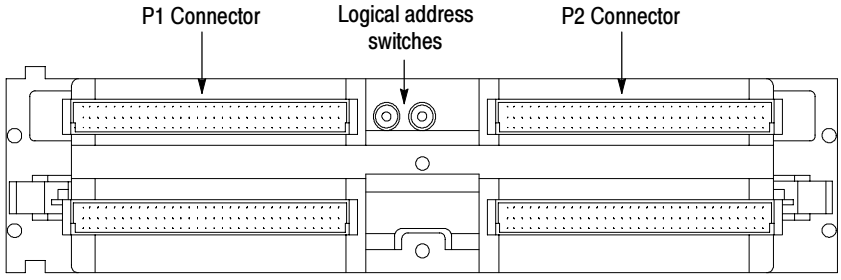


**Figure 2-7: Rear panel controls and connectors**

**P1 and P2 Connectors.** The acquisition board and the local processor unit (LPU) provide the electrical connections from the module to the mainframe. These electrical connections include power distribution, processor communications, and intermodule communications.

**Logical Address Switches.** The logical address switches determine the logical address of the module. These switches should normally be set to address FF. For more information on these switches and their settings, refer to *Logical Address* on page 2–1.

## Online Help

Most user information for operating the logic analyzer module is available through the online help within the logic analyzer application. You can select the online help from the pull-down help menu, by clicking the Help button in a dialog box, or by using the what's this help (click the question mark icon, drag the cursor to the item of interest on the screen, and then release the mouse button).

## Diagnostics

The logic analyzer module performs power-on diagnostics each time you power on the mainframe. The Calibration and Diagnostics property sheet appears at power-on if one or more of the diagnostics fail.

For more detailed tests, you can execute the extended diagnostics or the self calibration. For more information on the diagnostics, refer to *Calibration and Diagnostic Procedures* beginning on page 6–29.

***NOTE**. For best results, only run the diagnostics with the probes disconnected from the module.*

## Self Calibration

Self calibration is an internal routine that optimizes performance. No external equipment or user actions are required to complete the procedure. The logic analyzer saves the data generated by the self calibration in non-volatile memory.

***NOTE**. Performing the self calibration does not guarantee that all logic analyzer module parameters operate within limits. Operation within limits is achieved by performing the* Adjustment Procedures. *Proper operation may be confirmed by performing the performance verification procedures in this same manual.*

You can run the self calibration at any time during normal operation. To maintain measurement accuracy, perform the self calibration if more than one year has elapsed since the last self calibration.

You can check the status of the self calibration in the Calibration and Diagnostics property sheet.

If the logic analyzer module loses power during the self calibration, rerun the self calibration following the next power-on. The self calibration data generated before power was interrupted must be replaced with a complete set of new data. For best results, always perform the self calibration after at least a 30 minute warm-up.

The logic analyzer module may require several minutes to run the self calibration depending on the number of channels. Select Calibration and Diagnostics property sheet from the System menu. Select the Self Calibration tab page and select the logic analyzer module. Click on the Run button to start the self calibration. Upon completing the self calibration the logic analyzer module menu selection changes from Running to Calibrated.

## Menu Overview

The logic analyzer is controlled by interactive windows through the TLA application. The TLA application consists of the following windows:

- System Window. This window provides an overview of the entire logic analyzer. Use this window to navigate through the logic analyzer.

  The center of the System window displays icons that represent hardware modules installed in the logic analyzer. The icons are linked to the other windows in the logic analyzer.

- Setup Window. A setup window exists for each module in the logic analyzer. It contains all of the setup information for the logic analyzer module such as clocking, memory depth, threshold information, and channel information. Menus and dialogs contain information to set up the window as needed.

For the DSO, the Setup window contains setup information for each DSO channel such as the input voltage ranges, bandwidth, coupling, and termination. It also contains horizontal setup information and a link to the DSO Trigger window.

An External Oscilloscope setup window may be present if your logic analyzer connects to an external oscilloscope through the iView cable. This setup window provides setup, trigger, and connection information for oscilloscope and logic analyzer.

- Trigger Window. The Trigger window provides access to the logic analyzer module or DSO module trigger setups. For either module, you can specify various trigger events and trigger actions to help you capture the data that you are interested in.
- Listing Data Window. The Listing Data window displays acquired data as tabular text. Each column of data represents one group of data or other logical data information, such as time stamps. Each row of data represents a different time that the data was acquired; newer samples of data display below older samples.
- Waveform Data Window. The Waveform Data window displays acquired data as graphical waveforms. All defined channel groups display as busforms for the logic analyzer and as individual analog channels for the DSO module.
- On/Off Buttons. These buttons enable or disable the operation of the modules. Click the appropriate button to enable or disable the modules.

Refer to the online help for more information on the individual menus, icons, and fields within each window. You may also want to refer to the *Tektronix Logic Analyzer Family User Manual* for additional information.

# Merged Modules

The logic analyzer allows you to merge individual 102-channel or 136-channel module modules to provide a logic analyzer module with up to 680 channels. The following procedures provide information for merging and unmerging logic analyzer modules.

## Merging Rules

Before merging modules to create a merged module set, review the following guidelines.

- You can only merge 102-channel and 136-channel modules.
- You cannot merge TLA7Axx modules with TLA7Lx, TLA7Mx, TLA7Nx, TLA7Px, or TLA7Qx logic analyzer modules.
- Modules containing different memory depths can be merged, but will default to the shallowest memory depth being used.
- All modules in a merged set must have the same maximum clock rate.
- Modules must be physically adjacent and connected before you can merge them together in the System Configuration dialog box (see the instructions under *Merge Procedure*).
- You can merge two, three, four, or five modules together.
- The master module must have an equal or greater number of channels than the module(s) with which it is merged. If there is a second slave module, the Slave 1 must have an equal or greater number of channels as the Slave 2. Slave 3 cannot have more channels than the master module or Slave 1 and Slave 2. Slave 4 cannot have more channels than the master modules or any other slave modules.
- A merged module set can only reside in a single mainframe. You cannot merge modules across mainframes.
- To merge a module to an established merged module set, the established merged module set must be first unmerged through software via the System Configuration dialog box. Unmerged modules are the only potential candidates to add to a merged configuration.

## Merge Procedure

Complete the following steps to create a merged module from two or more individual modules. You must complete these steps prior to installing the modules in a mainframe.

***CAUTION.*** *To avoid damaging the mainframe or any modules, always power down the mainframe before removing or installing modules.*

1. Determine which modules will reside in the higher-numbered slots in a single mainframe. You will need to place the merge connector of these modules in the extended position. The module in the lowest-numbered slot must have the merge connector in the recessed position.

   Use Figure 2–8 as a guide for determining the location of the master module with the merged module set. Even though Figure 2–8 shows a five module set, you can still use the illustration to position the master module with respect to the slave module. For example, if you have a two module set, the master module is located in the lower-numbered slot, and the slave module is in the higher-numbered slot.

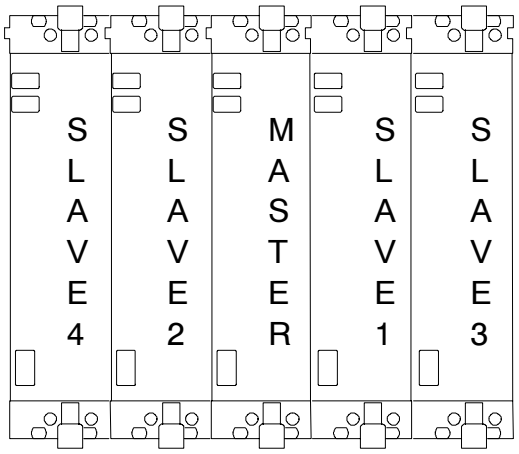


**Figure 2-8: Location of modules in a merged system**

2. Place the module on the right side.
3. Using a Torx T-10 screw driver, remove the two screws holding the merge connector to the module (see Figure 2–9).
4. Gently lift the merge connector out of the slot and place it in the extended position such that the screw holes line up over the two standoff posts.
5. Install the two screws into the standoff posts. Tighten the screws to 4-in. lbs.
6. Repeat steps 2 through 5 for the remaining modules.

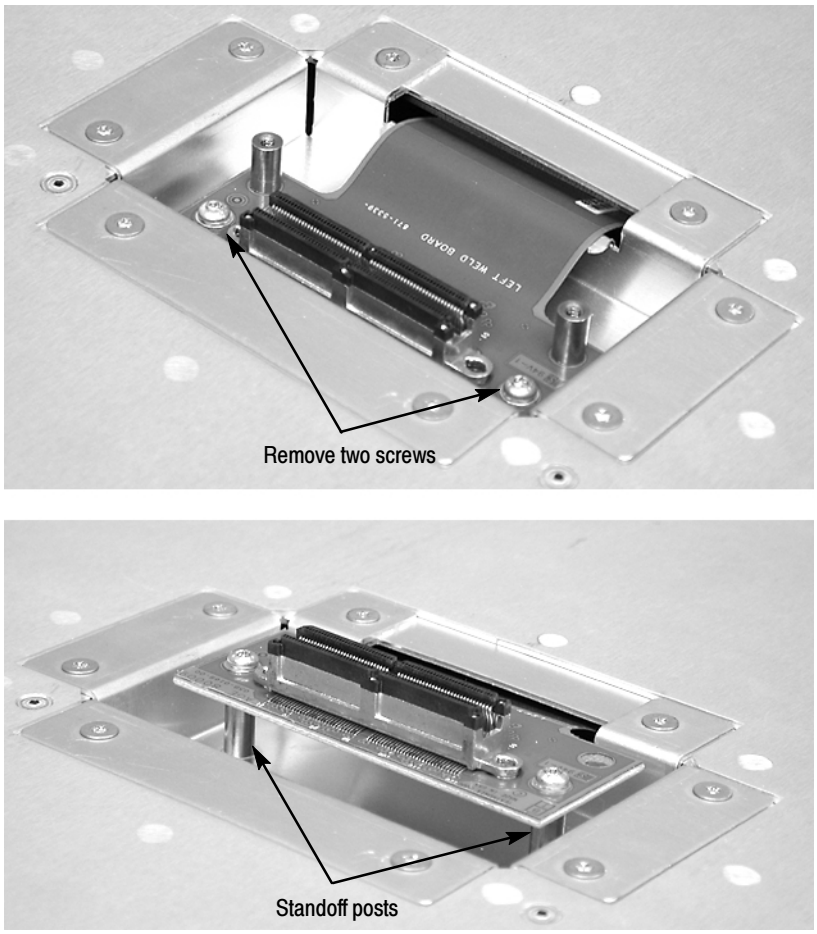


**Figure 2- 9: Removing the merge connector assembly from the module**

***NOTE****. When installing the merged modules into a mainframe, you may need the help of another individual.*

7. Place the first pair of  modules to be merged side-by-side such that the merge connector assemblies line up and connect between the two modules.
8. Push the two modules together until the connectors are seated in place.
9. Add any additional modules to the set.

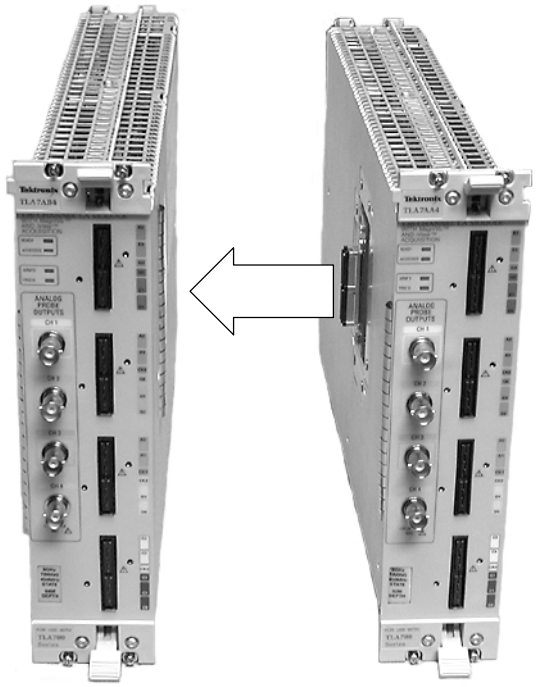

**Figure 2-10: Connecting the logic analyzer modules together**

***CAUTION.*** *Ensure that the mainframe is powered down before installing or removing the modules.*

**10.** Place the merged module set into the mainframe.

**11.** Align the tops and bottoms of the modules with the slots in the mainframe (see Figure 2–11 on page 2–18). You may need the help of another individual if your merged module set contains more than two modules.

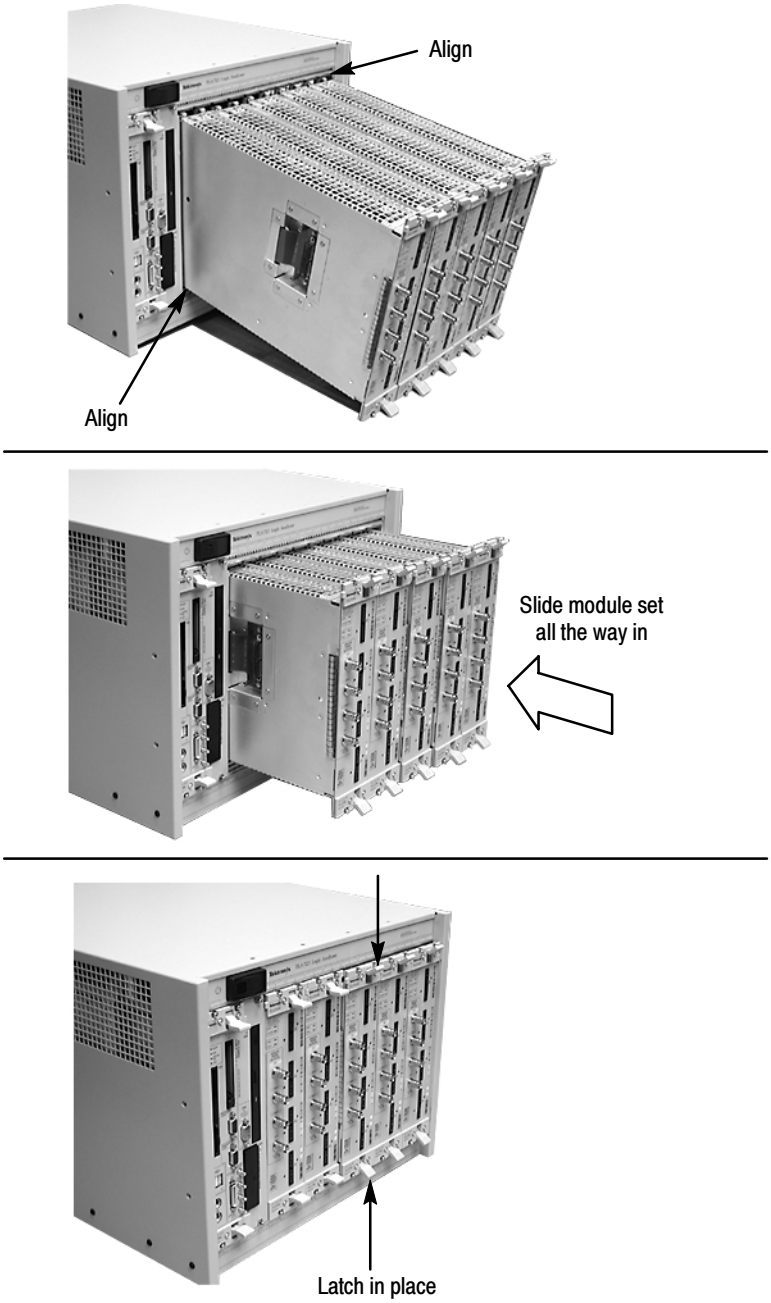


**Figure 2- 11: Installing the merged module set in the mainframe**

**12.** Slide the modules all the way into the mainframe until they rest against the rear panel connectors.

13. Use the injector handles to firmly seat the modules in place one at a time and then tighten the hold-down screws on each module. The merge cable assembly should allow enough play between two side-by-side modules.

14. After installing all of the modules, power on the mainframe and complete the merge process listed under the Merged Modules tab in the System Configuration dialog box.

## Unmerge Procedure

Although you can unmerge modules from a merged set from within the TLA application without physically separating modules, there will be times when you have to physically unmerge the modules. The following procedures provide the steps for unmerging the modules.

1. Power down the mainframe before removing the modules from the mainframe.

2. Use the ejector handles to disengage each module in the merged module set from the mainframe.

3. With the assistance of another individual, slide all of the merged modules out of the mainframe and place them on a static-free working surface.

4. Gently separate the modules on at a time from the merged module set.

5. Lay the modules on their right sides.

6. Remove the two Torx T-10 screws that hold the merge cable assembly to the module.

7. Place the merge cable assembly into the recessed position.

8. Install the two Torx T-10 screws onto the assembly and tighten the screws to 4 in-lbs.

9. Repeat steps 6 through 8 for the other modules.

You can now reinstall the modules in the mainframe as needed.

# Theory of Operation

This chapter describes the general operation of the logic analyzer module. This information is intended to help you isolate faults to the circuit board or probe level. It supplements diagnostic and troubleshooting information presented in the *Troubleshooting* section beginning on page 6–25.

The following *Block Level Description* describes circuit operation to the functional block level. Block diagrams are located in the *Diagrams* chapter beginning on page 9–1.

## Block Level Description

The block level description provides an overview of each functional circuit within the logic analyzer module. Except for the number of channels, the basic operation is the same for each individual module and for merged modules.

The basic logic analyzer module consists of two main circuit boards: the Local Processing Unit (LPU) board and the Acquisition board. Each circuit board has two connectors on the rear of the boards that provide connections to the mainframe.

Up to four active probes per module acquire data from the target system and send it to the logic analyzer module for processing. The logic analyzer module can use different types of probes (such as general purpose, high-density, or differential) depending on the user's application.

A single 102-channel or a 136-channel logic analyzer module can be merged with up to five modules to create a two-, three-, four-, or five-module-wide logic analyzer. The 34-channel and 68-channel modules do not support merging.

## Local Processor Unit (LPU) Board

The LPU board controls instrument hardware, signal acquisition, power conditioning, and communications functions. A 160-pin connector provides interconnections with the acquisition board for power supplies, data and control signals.

### Processor System

The processor system contains a microprocessor that controls the entire instrument. Commands and data sent to the instrument through the mainframe pass through the communications interface, which resides on the bus. The bus also routes data between the main processor system and the acquisition board.

The processor system includes the instrument firmware. To facilitate upgrades, the firmware resides in Flash ROM. The processor system also includes the nonvolatile RAM (NVRAM) used for the calibration constants, module serial numbers, and PowerFlex configuration information.

### Communications Interface

The Communications Interface transfers commands and data between the mainframe and the mainframe controller. Signals pass between the logic analyzer module and the mainframe through the rear connectors.

### Power Supplies

The onboard power supplies receive +5 V, –5.2 V, ±12 V, and ±24 V from the mainframe through the rear connectors. Voltage converters produce the +2.5 V supply for use on the acquisition board through the 160-pin connector between the LPU and acquisition board.

## Acquisition Board

The acquisition board accepts input signals from the probes and converts them to digital information. A 160-pin connector provides interconnections with the LPU board.

### Clock Circuitry

The system clock is derived from the 10 MHz clock from the backplane through a phase-locked loop. The acquisition run circuitry is integrated with the clock circuitry to support time correlation.

### Probe Interface

The probe interface consists of ASICs that receive data from the probes, compare the data against a threshold, and transfer the digital information to CMOS ASICs via differential outputs. Each ASIC in the probe interface receives 16 data channels and one clock channel. In addition to providing digital signals to the CMOS ASICs, the probe interface ASICs contain outputs for the Analog output signals.

### Analog Output Interface

The acquisition board has four SMA connectors that connect to the four BNC connectors on the front panel. The software (via the user interface) determines which signals will be sent to the four Analog output connectors. Regardless of the number of channels in the module, there will always be four signals available to route to the Analog output connectors.

### Power Supplies

Voltage converters produce the +3.3 V supply on the acquisition board and the ±3 V supplies for the active probes.

### Trigger and Storage Control Circuitry

Clocking and triggering is controlled by a single ASIC. This ASIC determines when acquisition data should be sampled based on the clock information and qualifier information. The ASIC also contains 16 Event resources for the purposes of word recognition, range recognition, and other trigger functions. In merged configuration, the ASIC communicates information between modules to ensure proper triggering.

### Acquisition Memory

The acquisition memory stores acquired data. The memory can be set up to store all data samples, or it can be split to store data samples and either glitch information or setup and hold violation information.

When the memory is split, only half the memory depth is available and can only run at half the speed. Every stored data sample takes up two memory locations, one to hold the actual data sample and the other to hold the corresponding glitch information or the setup and hold information.

Glitch storage is only enabled with asynchronous clocking while setup and hold storage is only enabled with synchronous clocking.

The trigger machine can trigger on either glitches or setup and hold violations without storing information. This allows the user to trigger on a glitch or on a setup and hold violation at maximum speed and maximum memory depth.

### Backplane Interface

The backplane interface provides the interface with the mainframe and the acquisition board. This interface contains intermodule signals that communicate to other modules in the logic analyzer mainframe. The interface also provides the 10 MHz reference clock for the clocking circuitry.

## Probes

The logic analyzer module connects to the target system through 34-channel probes (32 data channels and two clock/qualifier channels). Depending on the number of channels in the logic analyzer module, you can connect up to four logic analyzer probes to the module.

Currently three different types of active probes are supported for the logic analyzer module:

- P6860 34-channel high-density single-ended probe
- P6880 34-channel high-density differential probe
- P6810 34-channel general purpose probe

The two high-density probes connect directly to the circuit boards in the target system. The probe connections are footprints designed on the circuit boards. The footprints eliminate the need for additional electro-mechanical parts for probe connectors.

The general purpose probes have lead sets that connect to several general-purpose connectors on the target system.

Detailed information on the probes is available in the *P6810, P6860, & P6880 Logic Analyzer Probe Instruction Manual*.

## Merged Modules

A merged module consists of a Master module and one or more Slave modules connected together by a merge cable connector. Each module has its own merge cable connectors. The local bus sends the system clock of the Master module to the Slave modules. The merged modules must be located in adjacent slots.

The merge connector passes 48 signals between adjacent modules excluding the system clock. These signals consist of 16 trigger event signals, two storage control signals, 26 clock sample/control signals, and four data-login control signals.

# Performance Verification

This chapter contains procedures for functional verification, certification, and performance verification procedures for the logic analyzer modules. Generally, you should perform these procedures once per year or following repairs that affect certification.

***NOTE**. This chapter does not contain any procedures for verifying, adjusting, or certifying the TLACAL2 Performance Verification fixture. Please contact your local Tektronix service center for information on servicing the fixture.*

## Summary Verification

Functional verification procedures verify the basic functionality of the instrument inputs, outputs, and basic instrument actions. These procedures include power-on diagnostics, extended diagnostics, and manual check procedures. These procedures can be used for incoming inspection purposes.

Certification procedures certify the accuracy of an instrument and provide a traceability path to national standards. Calibration data reports are produced for the logic analyzer modules as output from the performance verification and adjustment software.

Performance verification procedures confirm that a product meets or exceeds the performance requirements for the published specifications documented in the *Specifications* chapter of this manual. Refer to Figure 4–1 on page 4–2 for a graphic overview of the procedures.

Adjustment procedures check for, and if necessary, correct any adjustment errors discovered when performing functional or performance verification procedures. The adjustment procedures for the logic analyzer modules are controlled by software but some of the adjustment procedures require manual intervention to move probes or to change test equipment settings.

The performance verification and adjustment software is provided on the product CD-ROM. If you have not already done so, refer to *Software Installation* beginning on page 2–7 for instructions on installing the software.

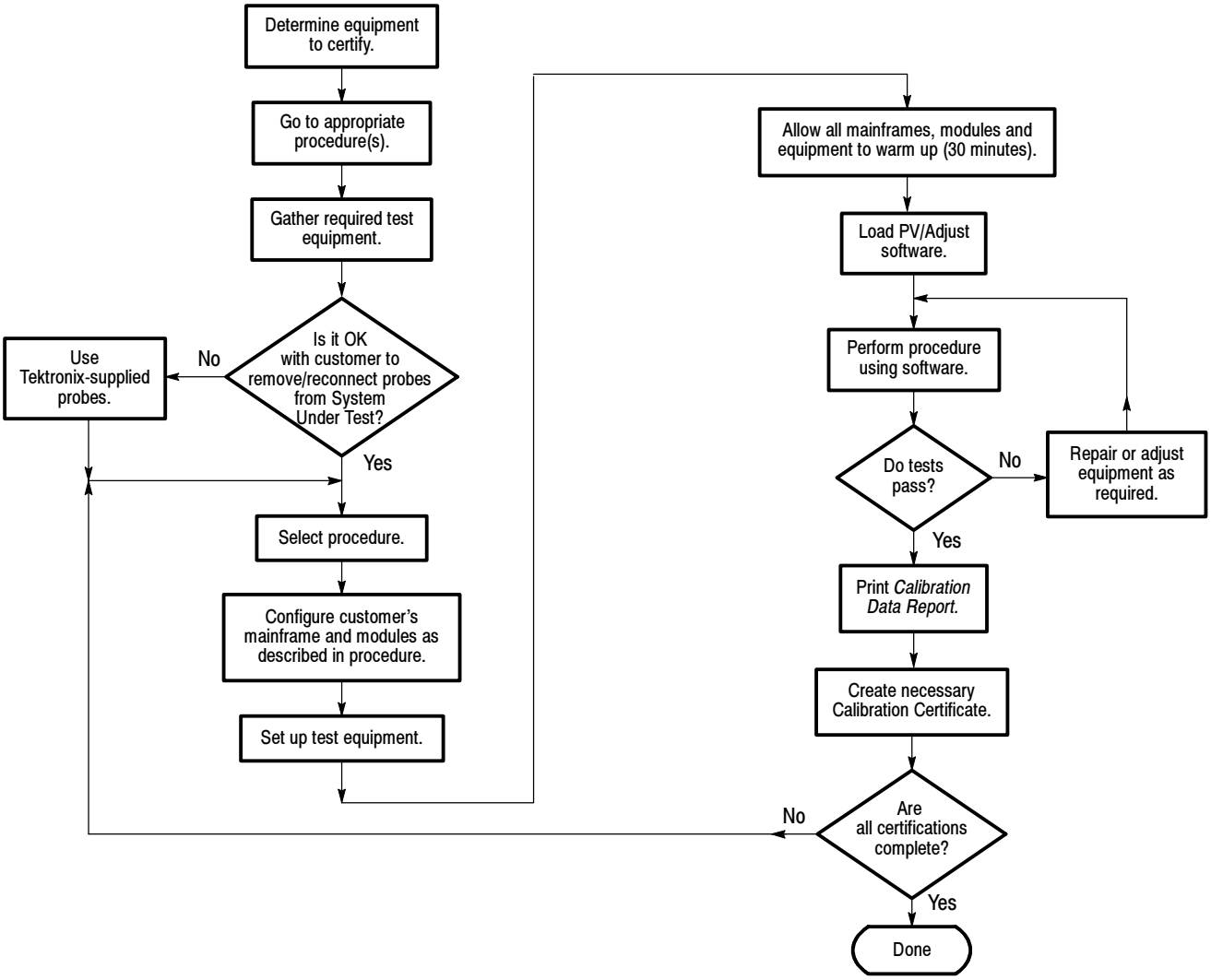


**Figure 4- 1: Calibration/certification procedure flow chart**

# Test Equipment

The procedures use external, traceable signal sources to directly test characteristics that are designated as checked (✓) in the *Specifications* chapter of this manual. Table 4–1 shows the required equipment list; this equipment is required for the performance verification and adjustment procedures.

**Table 4-1: Test equipment**

| Item number and description | Minimum requirements | Example |
|---|---|---|
| 1. Mainframe | TLA700 Series Mainframe with TLA Application software V4.2 or higher | TLA721 Benchtop Mainframe or<br>TLA715 Portable Mainframe |
| 2. Logic analyzer module with probes | TLA7Axx Series logic analyzer module | No substitute allowed |
| 3. Logic analyzer probes | P6810, P6860, or P6880 logic analyzer probes. One probe required for every 34-channels on the logic analyzer module | No substitute allowed |
| 4. Performance Verification test fixture with accessories | TLACAL2 test fixture; Includes:<br>4 Ribbon cables<br>4 Module interface connectors (MICs)<br>1 Probe interface connector (PIC)<br>4 P6041 BNC-to-SMB cables<br>8 MCX-to-MCX coaxial cables, with identification color bands | No substitute allowed |
| 5. Digital Multimeter with probes[1] | Agilent 34401A, 6.5 digit display, 35 ppm, 1 year accuracy, 1000 readings per minute, 100 nV sensitivity, GPIB controllable | No substitute allowed |
| 6. Oscilloscope[2] | Tektronix TDS694C Four channels, 3 GHz, 10GS/s | No substitute allowed |
| 7. USB-GPIB controller: | National Instruments 778195-01<br>Windows 2000 compatible with 2 m cable. | Tektronix iView cable |
| 8. GPIB cable | 2 m GPIB cable. | Tektronix part number 012-0991-00 |
| 9. RS-232 cable | 2 m RS-232 cable, 9-pin female-to-female connector | Tektronix part number 012-1379-00 |
| 10. BNC cables | 4 Analog Output BNC-to-BNC, low loss, 33 in. 10x cables | Tektronix part number 174-4595-00 |

**1 The digital multimeter is required to complete the Probe+PIC performance verification and adjustment procedure, the Module+MIC performance verification and adjustment procedures, the Module+Probe Gain & Offset performance verification procedures, and the certification procedures.**

**2 The oscilloscope is required to complete the performance verification procedures for the Analog Output tests.**

# Test Equipment Setup

The TLACAL2 Performance Verification and Adjustment fixture and other test equipment requires preliminary installation and setups. You will need the equipment listed in Table 4–1 on page 4–3 to complete the performance verification procedures. If you have not already installed the test fixture and test equipment, refer to *TLACAL2 Fixture Installation* on page 2–3 for the preliminary installation instructions.

Most of the individual procedures require specific test equipment setups depending on your logic analyzer configuration. These setups are listed prior to each test and are also described in the TLACAL2 software windows.

***CAUTION.*** *Always power down the TLACAL2 test fixture before connecting or disconnecting the ribbon cables. Failure to do so can damage the test fixture, the PIC, or the MICs.*

## Starting the Performance Verification Software

The performance verification software is a separate application that consists of executable software files. The software must be installed on the hard disk before you can use it; refer to *Software Installation* on page 2–7 for instructions on installing the software. You must quit the logic analyzer application before starting the performance verification software; you cannot run both applications at the same time.

Use the following steps to start and run the software. These steps are repeated under the individual procedures but are listed here to give you an overview of using the software.

1. Allow the logic analyzer and all test equipment to warm up for at least 30 minutes.
2. Exit the logic analyzer application.
3. Select Start → Programs → Tektronix Logic Analyzer → TLA7AxxPVAdjust (or double-click on the TLA7AxxPVAdjust icon on the desktop). An application window similar to Figure 4–2 appears.
4. Select the module that you want to test from the list and then click either the Verification button, Adjustment button, or Certification button depending on the type of procedure that you want to perform.


**Figure 4-2: Performance verification software startup window**

## Software Overview

After selecting the type of test that you want to run, a new dialog box appears. The dialog box contains the following information:

- Name, slot location, and serial number of the module to be tested
- Probe selection box
- A list of procedures organized by groups

The individual procedures are organized by groups that require the same test equipment setups. When moving between different groups, you will be asked to power down the test fixture, make the necessary connections In some cases, you will be asked to power down the test fixture, close the application, change the connections, and then restart the application.

Depending on the type of probe selected, the related procedures are indicated by a checkmark adjacent to the procedure. You can disable any procedures by clearing the procedure. All selected procedures will be tested beginning with the top-most procedure in the dialog box. In most cases, you will want to run all of the selected tests.

The software determines which GPIB instruments are required to perform the selected procedures and sets up the individual instruments. If any equipment problems are found, an appropriate error message will be displayed.

***NOTE.*** *Some of the procedures require a TDS694C oscilloscope and a Agilent 34401A digital multimeter connected to the logic analyzer via GPIB (see the footnotes in Table 4–1 for details). If you do not have the TDS694C oscilloscope or the digital multimeter connected to the GPIB, you cannot start the performance verification procedures that require those instruments.*

## Obtaining Test Results

After completing the various procedures, you have the option of saving the test results to a text file on the hard disk. You can assign a name to the file from a dialog box. You can then edit the file as necessary using any of the Windows tools or print the file.

## Troubleshooting

If any tests fail, use the following steps to troubleshoot the problems:

1. Check that all test equipment is powered on and has the proper warm-up time.
2. Check all test equipment for improper or loose connections.
3. Verify that the probes are properly connected to the logic analyzer module and that the retaining screws are tightened. The retaining screws must be tightened to provide a good ground connection for the probes.
4. Verify that all probes are properly connected to the test fixture. If you are using P6860 or P6880 probes, make sure that the alignment pin on the probe head is aligned with the hole on the test fixture. You must ensure a tight connection on the test fixture for these probes.
5. If you are using P6860 or P6880 probes, verify that the test fixture connections are clean and free of dust or dirt. If necessary, refer to the cleaning procedures in the *Maintenance* chapter.
6. Rerun mainframe or module diagnostics.
7. Run the self calibration for the module in question from the TLA application.
8. Run the adjustment procedures for the module in question.
9. Run the tests a second time to verify the failure.
10. If all else fails, contact your local Tektronix service center for additional information.

# Functional Verification

This section contains instructions for performing the functional verification procedures for the logic analyzer modules. These procedures provide an easy way to check the basic functionality of the logic analyzer modules and probes. The TLACAL2 test fixture or software is not required for any of the functional verification checks.

If any check within this section fails, refer to the Troubleshooting section in the *Maintenance* chapter of this manual for assistance. Failed tests indicate the instrument needs to be serviced.

The functional verification procedure consists of the following parts:

- Module self tests and power-on diagnostics
- Extended diagnostics
- Probe functional verification

This procedure provides a functional check only. If more detailed testing is required, perform the *Performance Verification Procedures* beginning on page 4–12 after completing this procedure.

Perform these tests whenever you need to gain confidence that the instrument is operating properly.

## Test Equipment

You will need the following equipment to complete the functional verification procedure:

- TLA700 Series logic analyzer mainframe with one logic analyzer module installed (more modules are required to check the merged functionality)
- At least one logic analyzer probe

## Setup

It is assumed that the logic analyzer module is properly installed in the mainframe. Refer to *Module Installation* on page 2–2 for module installation instructions.

Power on the logic analyzer mainframe and allow a 30-minute warm-up period before continuing with any procedures in this section.

## Module Self Tests and Power-On Diagnostics

During power-on, the installed modules perform an internal self test to verify basic functionality. No external test equipment is required. The self tests require only a few seconds per module to complete. The front-panel ARM'D and TRIG'D indicators blink during the self test. After testing completes, the front panel indicators have the following states:

- READY — Green (on)
- ACCESSED — off
- ARM'D — off
- TRIG'D — off

Next, the power-on diagnostics are run. If any self tests or power-on diagnostics fail, the instrument displays the Calibration and Diagnostics property sheet.

***NOTE**. If any diagnostics fail, you may need to run the self calibration before attempting to service the logic analyzer module. This may be especially true after you install the logic analyzer module in the mainframe for the first time. The Self Calibration procedure is listed under* Self Calibration *beginning on page 5–5.*

## Logic Analyzer Module Functional Verification Procedure

The following procedure checks the basic functionality of the logic analyzer module. You can perform this procedure with individual modules or with merged modules. Functional verification consists of running the extended diagnostics.

***NOTE**. Running the extended diagnostics invalidates any acquired data. If you want to save any of the acquired data, do so before running the extended diagnostics.*

Perform the following steps to complete the functional verification procedures:

1. Disconnect any probes connected to the logic analyzer module.
2. In the logic analyzer application, go to the System menu and select Calibration and Diagnostics.
3. Click the Extended Diagnostics tab.

4. Select the top level test and click the Run button.

   The diagnostics will perform each one of the tests listed in the menu under the module selection. All tests that displayed an Unknown status will change to a Pass or Fail status depending on the outcome of the tests.

5. Scroll through the test results and verify all tests pass.

***NOTE**. If the extended diagnostics fail, run the self calibration procedures as described under* Self Calibration *beginning on page 5–5 for the logic analyzer module under test and then rerun the extended diagnostics.*

## Probe Functional Verification

There are two ways of verifying probe functionality. One way is to connect the probes from the logic analyzer module to a signal source, adjust the appropriate threshold voltage levels, and then verify that the logic analyzer acquires the data in a listing or waveform window.

Alternately, you can perform the performance verification procedures which will verify that the logic analyzer and the attached probes meet or exceed the advertised specifications. The performance verification procedures are covered in the remainder of this chapter.

# Performance Verification Instructions

This section contains information to verify the performance of the logic analyzer module. Testing is performed using the performance verification software and the performance verification fixture.

As a general rule, these tests should be done once a year.

## Prerequisites

The performance verification procedures in this section comprise an extensive, valid confirmation of performance and functionality when the following requirements are met:

- The performance verification software must be loaded on the hard disk. Refer to *Software Installation* on page 2–7.
- The logic analyzer module must be installed in a mainframe and operating for at least 30 minutes at an ambient temperature between +20 °C and +30 °C.
- The TLACAL2 test fixture and other related test equipment must be installed, connected, and operating for at least 30 minutes at an ambient temperature between +20 °C and +30 °C.
- The logic analyzer module and the TLACAL2 test fixture must have been last adjusted at an ambient temperature between +20 °C and +30 °C.
- The logic analyzer and TLACAL2 test fixture must be in an operating environment within the limits described in the *Specifications* chapter of this manual.
- When verifying the performance of merged modules consisting of different types of individual modules, the merged module can be tested without separation. The performance verification software runs independent of the logic analyzer application and does not recognize configuration settings.
- If you are using P6860 probes or P6880 probes, you must use the thick board elastomers (available in the 020-2452-xx accessory kit). Refer to the *Operating Basics* chapter of the *P6810, P6860, & P6880 Logic Analyzer Probe Instruction Manual* for instructions on installing or changing the elastomers.

## Procedure Overview

When using the performance verification software, you will connect external test equipment and probes to the logic analyzer module in response to prompts on the screen. The software automatically selects the module settings and determines the results of each test.

The results of the tests are recorded in a temporary file and are available upon test completion for completing test records.

***NOTE**. Before testing an instrument following repair, you must first complete the adjustment procedure.*

Table 4–2 lists the specifications as checked (✓) in the *Specifications* chapter for the TLA7Axx logic analyzer modules and the TLA7Axx performance verification software checks used to verify those specifications. In addition to the software test listed in the table, some specifications are verified by the built-in diagnostics. By running all tests and diagnostics, you will verify the performance of the logic analyzer module and probes.

**Table 4-2: Performance verification tests**

| Specification | Test method |
|---|---|
| Threshold accuracy | Verified by the Thresholds test. Certified by running Certification procedure; refer to *Logic Analyzer Module Certification* beginning on page 4–30. |
| Channel-to-channel skew | Verified indirectly by the Setup and Hold window size procedure under Setup and Hold |
| Internal sampling period | Verified indirectly by Pulse Width procedure and time base Accuracy procedure |
| Minimum recognizable word (across all channels) | Verified indirectly by the Setup and Hold window size and by the Internal Sampling Period |
| Setup and hold window size (data and qualifiers) | Verified directly by Setup and Hold procedure (P6880 probe only) |
| Maximum synchronous clock rate | Diagnostics verify the clock detection/sampling circuitry. Bandwidth is verified by Setup and Hold procedures and by the Pulse Width procedure |
| Counters and timers | Verified by diagnostics |
| Trigger state sequence rate | Verified indirectly by the at-speed diagnostics and the Internal Sampling Period |

## Performance Verification Procedures

Table 4–3 provides a summary of the performance verification procedures. The procedures are listed by groups and include individual procedures. Some of these procedures are optional and are recommended for performing a thorough performance verification. Others are the minimum required to verify the advertised specifications of the logic analyzer module. Each group requires different equipment setups.

**Table 4-3: TLA7Axx performance verification procedures**

| Procedure by groups | Notes |
|---|---|
| Probe+PIC Procedure | Optional procedure; digital multimeter required; verifies probe only |
| Probe Gain and Offset | |
| Module+MIC Procedures | Optional procedures; digital multimeter required |
| Input Resistance | |
| Digital Gain and Offset | |
| Analog Gain and Offset | |
| Module+Probe Gain and Offset Procedures | Required procedures; digital multimeter required |
| Threshold[1] | |
| Analog Gain and Offset | |
| Module+Probe Timing Procedures | Required procedures |
| Pulse Width | |
| Timebase | |
| Analog Outputs to Oscilloscope | Optional procedure. TDS694C oscilloscope required |
| Setup and Hold Procedure | Can only be verified with P6860 high density logic analyzer probe |
| Setup and Hold | |

[1] **Certifiable parameter. This procedure can be run separate from the performance verification procedures. Select Certification button from main window in the software. The Certification instructions are listed on page 4-30.**

Use the tables and illustrations to set up and execute the procedures. The procedures assume that you have already installed the performance verification software on the logic analyzer mainframe. The procedures also assume that you will only perform the procedures selected in each group.

The procedures will vary depending on the type of probes that you have connected to the logic analyzer module and on the number of channels on your logic analyzer module.

Figure 4–3 shows the locations of connectors and test points on the performance verification fixture. You may need to refer to this illustration when connecting probes and cables to the fixture. You should also refer to the label on top of the test fixture.

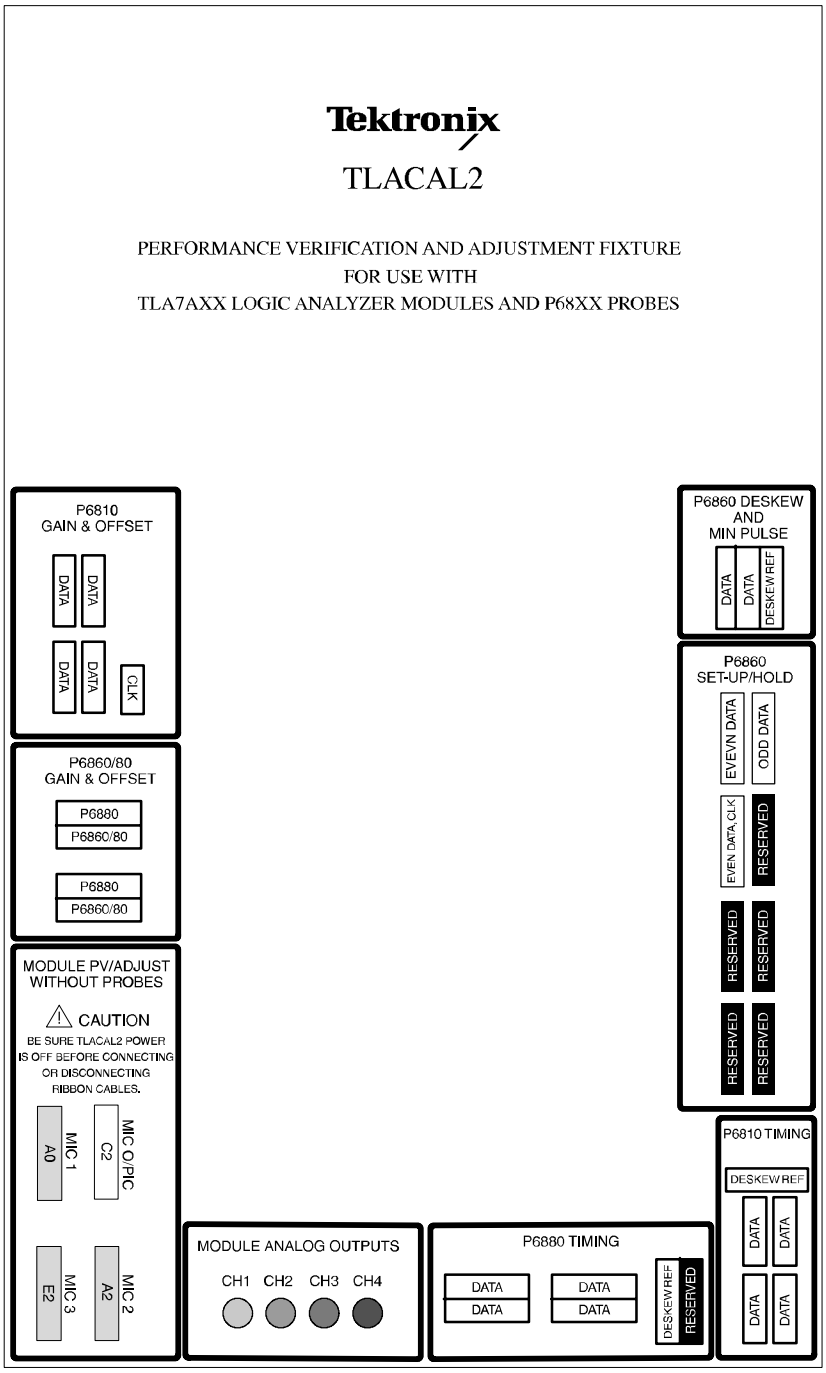


**Figure 4- 3: TLACAL2 test fixture connections**

## Probe+PIC Procedure

This procedure verifies probe gain and offset circuitry in the individual probes. This procedure is not dependent on any previous procedures. Use this procedure to verify the functionality of the probes. The procedure is optional and is not required to verify any module specifications.

The following procedure assumes that you will be testing one probe at a time without performing any other procedures.

**Equipment Setups.** It is assumed that the logic analyzer mainframe is already connected to the TLACAL2 test fixture and that the performance verification software is already installed on the hard disk of the logic analyzer. The following procedures describe the specific connections from the probes and to the test fixture.

***CAUTION.*** *If you have any P6041cables connected from the logic analyzer to the TLACAL2 test fixture, always disconnect one end of each P6041 cable before powering down the test fixture.*

*Always power down the test fixture before connecting or disconnecting ribbon cables. Failure to do so can damage the test fixture, the PIC, or the MICs.*

1. Power down the TLACAL2 test fixture before connecting the ribbon cables and the (PIC).

***CAUTION.*** *To avoid damaging the test fixture and the PICs through static discharge, always wear a grounded antistatic wrist strap. Avoid handling individual components of the test fixture without static protection.*

2. Connect one of the ribbon cables to the MIC0/PIC connector (J141) on the test fixture.
3. Connect the PIC to the other end of the ribbon cable.
4. Connect any one of the coaxial cables from the TV (test voltage) connectors on the test fixture to the TV connector on the PIC.
5. Connect the multimeter leads to the DMM test points (J390) on the test fixture. Connect the positive lead to the + connector and the negative (ground) lead to the – connector.
6. Connect the probe to be tested to the PIC.
7. If you are adjusting a P6810 probe:
   a. Connect the lead sets to the P6810 GAIN & OFFSET Data connections at J100, J101, J110, and J111 on the test fixture.

**b.** Connect the clock/qualifier leads to the SNGL square pins at J220. Make sure that you connect the ground side or the "-" side to the square pins with the GND label.

**8.** If you are testing a P6860 probe, connect the probe heads to the P6860/80 GAIN & OFFSET connections at J120 and J130 on the test fixture. If you are testing a P6880 probe, connect the probe heads at J120, J121, J130, and J131 on the test fixture.

---

***NOTE.*** *Make sure that the alignment pin on the P6860 or P6880 probe head is aligned with the hole on the test fixture. Tighten the probe head screws by alternating between them until they are finger tight (no more than 1 in-lbs of torque).*

---

**9.** Power on the test fixture, logic analyzer mainframe, and allow all test equipment to warm up for 30 minutes before continuing.

**Start the Software.** Complete the following steps to start the performance verification software and to run the verification procedures:

**1.** Exit the TLA application on the logic analyzer.

**2.** Double-click the TLA7Axx Performance Verification icon on the desktop to open the application (see Figure 4–2 on page 4–5).

**3.** Click the Verification button to start the software. A Verification dialog box similar to Figure 4–4 appears.

**4.** Select the probe type near the bottom of the dialog box.

**5.** Select the Probe Gain & Offset procedure (the default setting is not checked) and clear any other procedures.

---

***NOTE.*** *The software will perform all selected procedures in the listed sequence. To limit the test to specific procedures, clear any procedures that you do not want to run.*

---

**6.** Click the Next button at the bottom of the dialog box to begin the procedure.

A list of connection instructions displays for the current procedure.

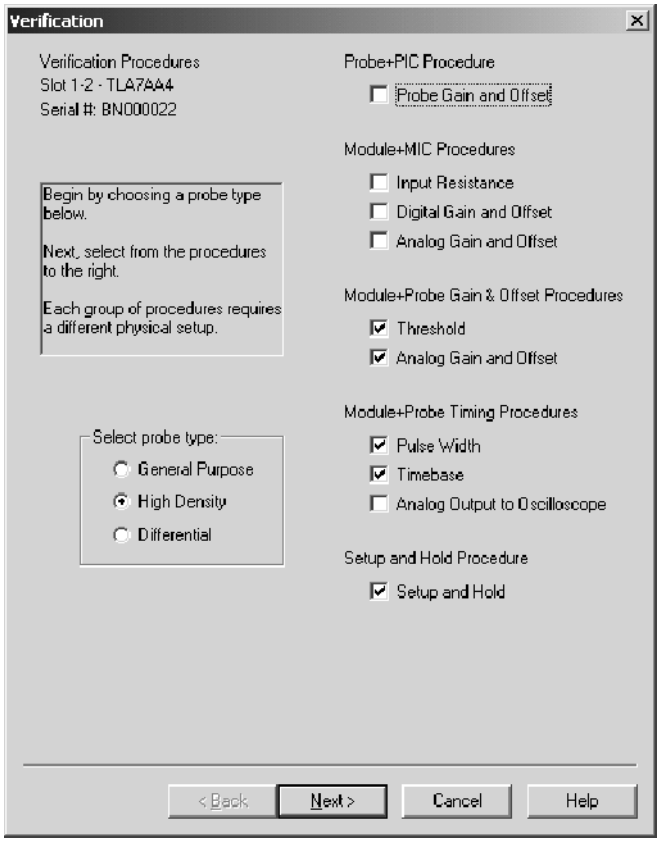


**Figure 4- 4: Default Verification dialog box**

**7.** Verify that your connections match those of the instructions. Then click the Next button to begin the procedure.

The software will begin the verification procedures and display a list of test results in the window.

**8.** After the procedure finishes, click the Next button to open the Finish dialog box where you can save the results to a file. Enter a file name and click the Save button. You can use the Save dialog to save the file to a folder of your choice or use the default location.

**9.** If you are testing more than one probe, disconnect the first probe and connect the next probe. There is no need to power down the test fixture while changing probes.

**10.** Click the Back button to return to the instructions dialog.

**11.** Click the Next button to test the next probe.

12. After completing the last probe, you can exit the application or return to the main window to perform other procedures.

***CAUTION.*** *Power down the test fixture before disconnecting the PIC from the test fixture. Failure to do so can damage the test fixture or the PIC.*

## Module+MIC Procedures

These procedures verify the input resistance, the digital gain and offset, and the analog gain and offset parameters of the logic analyzer probe input sections. These procedures are performed without the logic analyzer probes. The procedures are optional and do not verify any advertised specifications. However, they are helpful in verifying the logic analyzer functionality and for troubleshooting purposes.

**Equipment Setups.** It is assumed that the logic analyzer is already connected to the TLACAL2 test fixture and that the performance verification software is already installed on the hard disk of the logic analyzer. It is also assumed that the logic analyzer module is installed in the logic analyzer mainframe. The following procedures describe the specific connections from the logic analyzer module to the MICs and to the TLACAL2 test fixture.

***CAUTION.*** *If you have any P6041cables connected from the logic analyzer to the TLACAL2 test fixture, always disconnect one end of each P6041 cable before powering down the test fixture.*

*Always power down the test fixture before connecting or disconnecting ribbon cables. Failure to do so can damage the test fixture, the PIC, or the MICs.*

1. Power down the TLACAL2 test fixture before connecting the ribbon cables and the MICs.

***CAUTION.*** *To avoid damaging the test fixture, the PIC, or the MICs through static discharge, always wear a grounded antistatic wrist strap. Avoid handling individual components of the test fixture without static protection.*

2. Connect the four ribbon cables to the ribbon cable connectors on the test fixture.
3. Disconnect the PIC if it is connected to the ribbon cable.
4. Connect a MIC to each of the ribbon cables.
5. Connect any one of the coaxial cables from the CS (current source) connectors on the test fixture to the CS connector on the MIC.

6. Connect any one of the coaxial cables from the TV (test voltage) connectors on the test fixture to the TV connector on the MIC.
7. Connect the multimeter leads to the DMM test points (J390) on the test fixture. Connect the positive lead to the + connector and the negative (ground) lead to the - connector.
8. Connect a P6041 cable from each of the Analog Output BNC connectors to the corresponding connector on the front of the test fixture (if necessary, refer to the label on the test fixture for the connection locations).
9. Connect the ribbon cables with the MICs to the appropriate connector on the logic analyzer module.
10. Power on the test fixture and the logic analyzer and allow a 30 minute warm-up period.

**Start the Software.** Complete the following steps to start the software:

1. Exit the TLA application on the logic analyzer.
2. Double-click the TLA7Axx Performance Verification icon on the desktop. An application window similar to Figure 4-2 on page 4-5 appears.
3. If you have more than one logic analyzer module in your mainframe, select the logic analyzer module to be verified from the list in the window.
4. Click the Verification button to start the software. A Verification dialog box similar to Figure 4-4 on page 4-17 appears.
5. Select Input Resistance, Digital Gain and Offset, and Analog Gain and Offset and clear any other procedures.

---

***NOTE**. The software will perform all selected procedures without interruption. To limit the test to specific procedures, clear any procedures that you do not want to run.*

---

6. Click the Next button at the bottom of the dialog box to begin the procedure.

   A list of connection instructions displays for the current procedure.
7. Verify that your connections match those of the instructions. Then click the Next button to begin the procedures.

   The software will begin the verification procedures and display a list of results in the window.

8. After the procedure finishes, click the Next button to open the Finish dialog box where you can save the results to a file. Enter a file name and click the Save button. You can use the Save dialog to save the file to a folder of your choice or use the default location.

9. Click the Finish button to finish the procedure and return to the startup window.

***CAUTION.*** *Always disconnect one end of each P6041 cable before powering down the TLACAL2 test fixture. Failure to do so can damage the test fixture.*

10. Disconnect one end of each P6041 cable before powering down the TLACAL2 test fixture.

## Module+Probe Gain and Offset Procedures

These procedures verify the analog gain and offset parameters of the logic analyzer module. These procedures require you to connect the logic analyzer probes to the test fixture; the actual connections depend on the type of probe and the number of channels of your logic analyzer module. The procedures also verify the Threshold specifications of the logic analyzer module; this is a certifiable parameter.

**Equipment Setups.** It is assumed that the logic analyzer is already connected to the TLACAL2 test fixture and that the performance verification software is installed on the hard disk of the logic analyzer. It is also assumed that the logic analyzer module is installed in the logic analyzer mainframe. The following procedures describe the specific connections from the logic analyzer module to the probes and to the TLACAL2 test fixture.

***CAUTION.*** *Always power down the TLACAL2 test fixture before connecting or disconnecting the ribbon cables. Failure to do so can damage the test fixture, the PIC, or the MICs.*

*There is no need to power down the test fixture if you are only connecting probes, the P6041 cables, or the digital multimeter to the test fixture.*

1. Connect a P6041 cable from each of the Analog Output BNC connectors to the corresponding connector on the front of the test fixture (if necessary, refer to the label on the test fixture for the connection locations).

2. Connect the multimeter leads to the DMM test points (J390) on the test fixture. Connect the positive lead to the + connector and the negative (ground) lead to the – connector.

3. Connect a logic analyzer probe from the logic analyzer C0/C1/C2/C3 input connector (or the C3/C2/A3/A2 connector for 34- or 68-channel modules) to the appropriate connectors on the test fixture as described in the following steps.

4. If you are using a P6810 probe:

   a. Connect the lead sets to the P6810 GAIN & OFFSET Data connections at J100, J101, J110, and J111 on the test fixture.

   b. Connect the clock/qualifier leads to the SNGL square pins at J220. Make sure that you connect the ground side or the "–" side to the square pins with the GND label.

5. If you are using a P6860 probe, connect the probe heads to the P6860/80 GAIN & OFFSET connections at J120 and J130 on the test fixture. If you are testing a P6880 probe, connect the probe heads at J120, J121, J130, and J131 on the test fixture.

---

***NOTE**. Make sure that the alignment pin on the P6860 or P6880 probe head is aligned with the hole on the test fixture. Tighten the probe head screws by alternating between them until they are finger tight (no more than 1 in-lbs of torque).*

---

6. Power on the test fixture, logic analyzer, and the other test equipment. Allow all test equipment to warm up for 30 minutes before continuing the procedure.

**Start the Software.** Complete the following steps to start the software and to run the procedures:

1. Exit the TLA application on the logic analyzer.

2. Double-click the TLA7Axx Performance Verification icon on the desktop. An application window similar to Figure 4–2 on page 4–5 appears.

3. If you have more than one logic analyzer module in your mainframe, select the logic analyzer module from the list in the window.

4. Click the Verification button to start the software. A Verification dialog box similar to Figure 4–4 on page 4–17 appears.

5. Select the probe type near the bottom of the dialog box.

6. Verify that Threshold and Analog Gain and Offset are selected under Module+Probe Gain & Offset Procedures. Clear all other procedures in the dialog box.

***NOTE**. The software will perform all selected procedures in the listed sequence. To limit the test to specific procedures, clear any procedures that you do not want to run. If you want to run all of the selected procedures, you will need to play close attention to the connection instructions as they appear on the screen.*

**7.** Click the Next button at the bottom of the dialog box to begin the procedure.

A list of connection instructions displays for the procedure.

***NOTE**. Some of the connection information may vary depending on the configuration of your logic analyzer module. The connection information in the window should track your logic analyzer module; the printed instructions in this section may differ because they assume you are testing a 136-channel module.*

**8.** Verify that your connections match those of the instructions. Then click the Next button to begin the procedure.

The software will begin the procedures and display a list of results in the window.

**9.** After the first set of procedures are done, click the Next button to display the instructions for the next step. In most cases you only need to connect a different probe to the test fixture.

**10.** After changing the connections, click the Next button to continue the procedures.

**11.** Repeat steps 8 through 9 as indicated by the software.

**12.** After the procedure finishes, click the Next button to open the Finish dialog box where you can save the results to a file. Enter a file name and click the Save button. You can use the Save dialog to save the file to a folder of your choice or use the default location.

**13.** Click the Finish button to complete the process.

***CAUTION.** Always disconnect one end of each P6041 cable before powering down the TLACAL2 test fixture. Failure to do so can damage the test fixture.*

**14.** Disconnect one end of each P6041 cable before powering down the TLACAL2 test fixture.

## Module+Probe Timing Procedures

These procedure verify the minimum pulse width specification, the accuracy of the time base, and the analog output path.

***NOTE**. The Analog Output to Oscilloscope procedure is an optional procedure. You can only perform this procedure if you have a TDS694C oscilloscope connected to the analog outputs of the logic analyzer module; no other oscilloscopes can be used.*

**Equipment Setups.** It is assumed that the logic analyzer is already connected to the TLACAL2 test fixture and that the performance verification software is installed on the hard disk of the logic analyzer. It is also assumed that the logic analyzer module is installed in the logic analyzer mainframe. The following procedures describe the specific connections from the logic analyzer module to the probes and the TLACAL2 test fixture.

***CAUTION.** If you have any P6041cables connected from the logic analyzer to the TLACAL2 test fixture, always disconnect one end of each P6041 cable before powering down the test fixture.*

*Always power down the test fixture before connecting or disconnecting ribbon cables. Failure to do so can damage the test fixture, the PIC, or the MICs.*

1. Connect a probe to each probe connector on the logic analyzer module.
2. Refer to Table 4–4 on page 4–24 and to Figure 4–5 on page 4–25 to connect the probe from the logic analyzer C0/C1/C2/C3 input connector (or the C3/C2/A3/A2 connector if you have a 34- or 68-channel module) to the appropriate connectors on the test fixture.

***NOTE**. Make sure that the alignment pin on the P6860 or P6880 probe head is aligned with the hole on the test fixture. Tighten the probe head screws by alternating between them until they are finger tight (no more than 1 in-lbs of torque).*

3. If you are using a P6810 probe, make sure that you connect the ground or low side of the lead sets to the GND side of the connectors on the test fixture. Connect the clock/qualifier leads to the DESKEW REF connector; make sure that you connect the ground side or the "–" side to the square pins with the GND label. The single ground lead does not need to be connected.

**Table 4-4: Module+Probe Timing procedure probe connections**

| Probe | TLACAL2 test fixture connections |
|---|---|
| P6810 | P6810 TIMING<br>(J881, J882, J883, J884 data connectors<br>J880 Deskew Ref connector) |
| P6860 | P6860 DESKEW AND MIN PULSE<br>(J610, J611 data connectors<br>J612 deskew ref connector) |
| P6880 | P6880 TIMING<br>(J581, J582, J583, J584 data connectors,<br>J680 Deskew Ref connector) |

4. If you are going to perform the Analog Output to Oscilloscope procedure, connect the BNC-to-BNC cable from each of the Analog Output BNC connectors on the logic analyzer module to the corresponding inputs on the oscilloscope.

5. Power on the test fixture, logic analyzer, and oscilloscope and allow all test equipment to warm up for 30 minutes before continuing the procedure.

**Start the Software.** Complete the following steps to start the software and to run the procedures:

1. Exit the TLA application on the logic analyzer.

2. Double-click the TLA7Axx Performance Verification icon on the desktop. An application window similar to Figure 4–2 on page 4–5 appears.

3. If you have more than one logic analyzer module in your mainframe, select the logic analyzer module from the list in the window.

4. Click the Verification button to start the software. A Verification dialog box similar to Figure 4–4 on page 4–17 appears.

5. Select the probe type near the bottom of the dialog box.

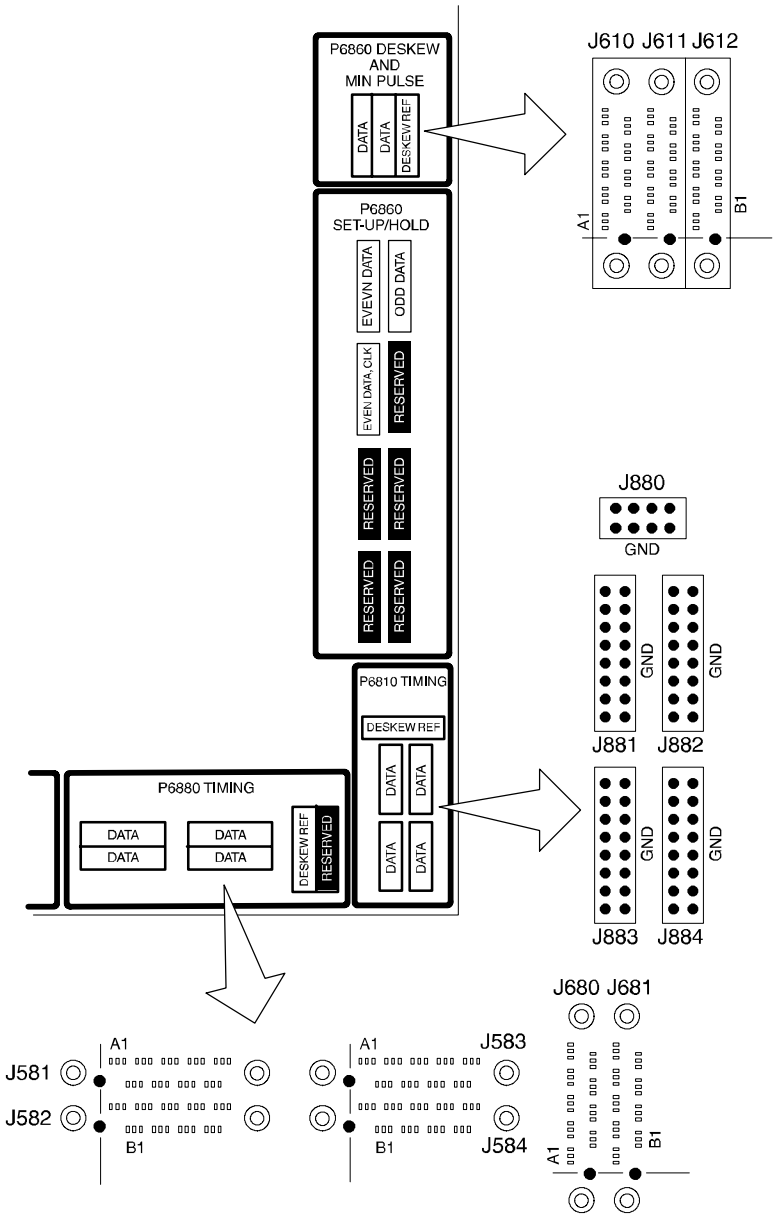


**Figure 4- 5: Module+Probe timing procedure probe connections**

6. Verify that Pulse Width and Timebase are selected under Module+Probe Timing Procedures.

7. If you want to perform the analog output procedure, select the Analog Output to Oscilloscope (it is not checked).

8. Clear all other procedures in the dialog box.

***NOTE**. The software will perform all selected procedures without interruption. To limit the test to specific procedures, clear any procedures that you do not want to run. If you want to run all of the selected procedures, you will need to play close attention to the connection instructions as they are displayed on the screen.*

**9.** Click the Next button at the bottom of the dialog box to begin the procedure.

A list of connection instructions displays for the first procedure.

***NOTE**. Some of the connection information may vary depending on the configuration of your logic analyzer module. The connection information in the window should track your logic analyzer module; the printed instructions in this section may differ because they assume you are testing a 136-channel module.*

**10.** Verify that your connections match those of the instructions. Then click the Next button to begin the procedure.

The software will begin the procedures and display a list of results in the window.

***NOTE**. The pulse width test may show failures at the initial threshold settings. However, the test will automatically rerun at other threshold settings where it looks for an overall "pass" at a threshold. You can view the overall pass/fail result at the top of the results for the pulse width test.*

**11.** After the first set of procedures are done, click the Next button to display the instructions for the next step. In most cases you only need to connect a different probe to the test fixture.

**12.** After changing the connections, click the Next button to continue the procedures.

**13.** Repeat steps 8 through 9 as indicated by the software.

**14.** When the software is ready to start the Analog Output to Oscilloscope procedure, a dialog appears on the screen. This dialog gives you three choices about pausing the procedure. Select one of the options to either pause on failures, pause on every step, or do not pause on any steps (default selection). Then click the Next button to continue.

***NOTE**. Selecting one of the pause options allows you to manually check the oscilloscope display for pass or fail information. You will not be able to change the pause options until the entire procedure is complete.*

15. After the procedure finishes, click the Next button to open the Finish dialog box where you can save the results to a file. Enter a file name and click the Save button. You can use the Save dialog to save the file to a folder of your choice or use the default location.

16. Click the Finish button to complete the process.

## Setup and Hold Procedure

This procedure verifies the setup and hold specification of the logic analyzer module. This procedure can only be verified with the P6860 probes. The procedure requires several iterations of connecting and disconnecting probes to the TLACAL2 test fixture.

**Equipment Setups.** It is assumed that the logic analyzer is already connected to the TLACAL2 test fixture and that the performance verification software is installed on the hard disk of the logic analyzer. It is also assumed that the logic analyzer module is installed in the logic analyzer mainframe. The following procedures describe the specific connections from the logic analyzer module to the probes and the TLACAL2 test fixture.

1. Connect the probes to the logic analyzer.

2. Connect probe from the logic analyzer A3/A2/CK0 input connector to the P6860 SETUP & HOLD area (J630) on the test fixture (see Figure 4–6 on page 4–28 if necessary).

---

***NOTE**. Make sure that the alignment pin on the P6860 probe head is aligned with the hole on the test fixture. Tighten the probe head screws by alternating between them until they are finger tight (no more than 1 in-lbs of torque).*

---

3. Connect probe from the logic analyzer E1/E0/QL2 input connector to the P6860 SETUP & HOLD area (J620) on the test fixture (see Figure 4–6 on page 4–28 if necessary).

4. Connect probe from the logic analyzer E3/E2/QL3 input connector to the P6860 SETUP & HOLD area (J621) on the test fixture (see Figure 4–6 on page 4–28 if necessary).

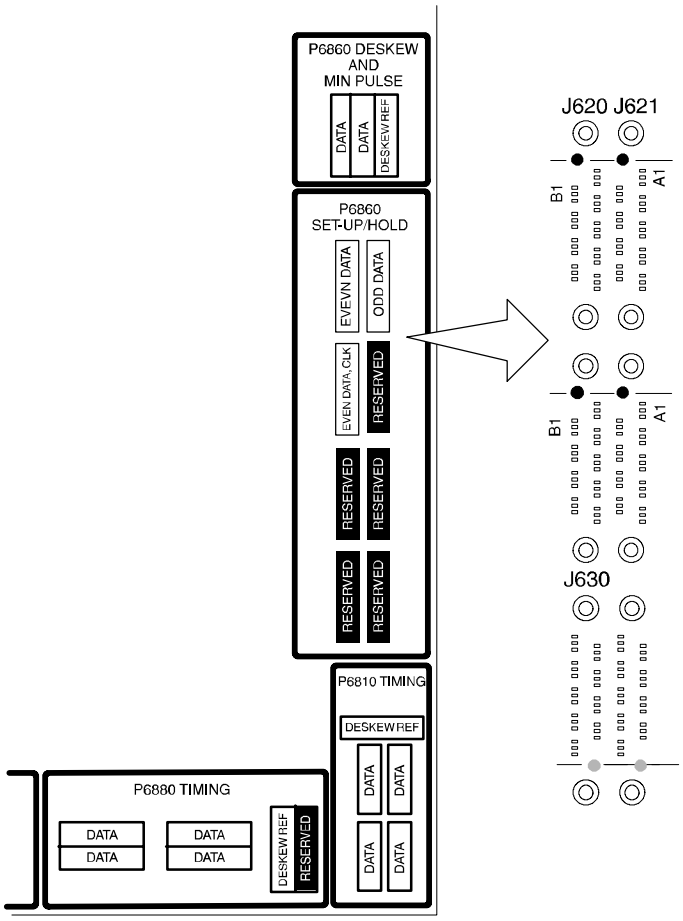


**Figure 4- 6: P6860 Setup & Hold procedure connections**

**5.** Power on the test fixture, logic analyzer, and oscilloscope and allow all test equipment to warm up for 30 minutes before continuing the procedure.

**Start the Software.** Complete the following steps to start the software and to run the procedures:

1. Exit the TLA application on the logic analyzer.
2. Double-click the TLA7Axx Performance Verification icon on the desktop. An application window similar to Figure 4–2 on page 4–5 appears.
3. If you have more than one logic analyzer module in your mainframe, select the logic analyzer module from the list in the window.
4. Click the Verification button to start the software. A Verification dialog box similar to Figure 4–4 on page 4–17 appears.
5. Verify that Setup and Hold is selected under Setup and Hold Procedures.
6. Clear all other procedures in the dialog box.

***NOTE**. The software will perform all selected procedures without interruption. To limit the test to specific procedures, clear any procedures that you do not want to run. If you want to run all of the selected procedures, you will need to play close attention to the connection instructions as they are displayed on the screen.*

7. Click the Next button at the bottom of the dialog box to begin the procedure.

   A list of connection instructions displays for the procedure.

***NOTE**. Some of the connection information may vary depending on the configuration of your logic analyzer module. The connection information in the window should track your logic analyzer module; the printed instructions in this section may differ because they assume you are testing a 136-channel module.*

8. Verify that your connections match those of the instructions. Then click the Next button to begin the procedure.

   The software will begin the procedures and display a list of results in the window.
9. After the first set of procedures are done, click the Next button to display the instructions for the next step. Move the probes on the test fixture as indicated by the instructions.
10. After changing the connections, click the Next button to continue the procedures.
11. Repeat steps 8 through 9 as indicated by the software.

12. After the procedure finishes, click the Next button to open the Finish dialog box where you can save the results to a file. Enter a file name and click the Save button. You can use the Save dialog to save the file to a folder of your choice or use the default location.

13. Click the Finish button to complete the process.

## Logic Analyzer Module Certification

This section describes the procedures to certify the logic analyzer. You can certify the logic analyzer without completing the main performance verification procedures. Table 4–5 lists the certifiable parameters for the logic analyzer.

**Table 4-5: Logic analyzer certification test**

| Performance verification test name | Specification tested |
|---|---|
| 1. Thresholds[1] | Threshold accuracy |

[1] **Certifiable parameter**

To certify the logic analyzer module, use the performance verification software and click the Certification button. Perform the required procedure and then print the results to obtain a copy of the software-generated calibration data report.

***NOTE****. The certification procedures have the same prerequisites as the performance verification procedures. Refer to* Prerequisites *on page 4–10 for a detailed list of prerequisites.*

### Equipment Setups

These procedures require the same setups as described for the Performance Verification procedures. It is assumed that the logic analyzer is already connected to the TLACAL2 test fixture and that the performance verification software is installed on the hard disk of the logic analyzer. It is also assumed that the logic analyzer module is installed in the logic analyzer mainframe. The following procedures describe the specific connections from the logic analyzer module to the probes and the TLACAL2 test fixture.

***CAUTION.*** *If you have any P6041cables connected from the logic analyzer to the TLACAL2 test fixture, always disconnect one end of each P6041 cable before powering down the test fixture.*

*Always power down the test fixture before connecting or disconnecting ribbon cables. Failure to do so can damage the test fixture, the PIC, or the MICs.*

*However, there is no need to power down the test fixture if you are only connecting probes, the P6041 cables, or the digital multimeter.*

1. Connect a P6041 cable from each of the Analog Output BNC connectors to the corresponding connector on the front of the test fixture (if necessary, refer to the label on the test fixture for the connection locations).
2. Connect the multimeter leads to the DMM test points (J390) on the test fixture. Connect the positive lead to the + connector and the negative (ground) lead to the – connector.
3. Connect a logic analyzer probe from the logic analyzer C0/C1/C2/C3 input connector (or the C3/C2/A3/A2 connector if you have a 34- or 68-channel module) to the appropriate connectors on the test fixture.
4. If you are using a P6810 probe:
   a. Connect the lead sets to the P6810 GAIN & OFFSET Data connections at J100, J101, J110, and J111 on the test fixture.
   b. Connect the clock/qualifier leads to the SNGL square pins at J220. Make sure that you connect the ground side or the "–" side to the square pins with the GND label.
5. If you are using a P6860probe, connect the probe heads to the P6860/80 GAIN & OFFSET connections at J120 and J130 on the test fixture. If you are using a P6880 probe, connect the probe heads to J120, J121, J130, and J131 on the test fixture.

***NOTE****. Make sure that the alignment pin on the P6860 probe head is aligned with the hole on the test fixture. Tighten the probe head screws by alternating between them until they are finger tight (no more than 1 in-lbs of torque).*

6. Power on the test fixture, logic analyzer, and other test equipment. Allow all test equipment to warm up for 30 minutes before continuing.

## Start the Software

Complete the following steps to start the software and to run the procedures:

1. Exit the TLA application on the logic analyzer.
2. Double-click the TLA7Axx Performance Verification icon on the desktop. An application window similar to Figure 4–2 on page 4–5 appears.
3. If you have more than one logic analyzer module in your mainframe, select the logic analyzer module from the list in the window.
4. Click the Certification button to start the software. A Certification dialog box similar to Figure 4–7 appears.
5. Select the probe type near the bottom of the dialog box.

   The Threshold Certification Procedure is selected by default.
6. Click the Next button at the bottom of the dialog box to begin the procedure.

   A list of connection instructions displays for the procedure.

---

***NOTE.*** *Some of the connection information may vary depending on the configuration of your logic analyzer module. The connection information in the window should track your logic analyzer module; the printed instructions in this section may differ because they assume you are testing a 136-channel module.*

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7. Verify that your connections match those of the instructions. Then click the Next button to begin the certification procedure.

   The software will begin the procedures and display a list of results in the window.

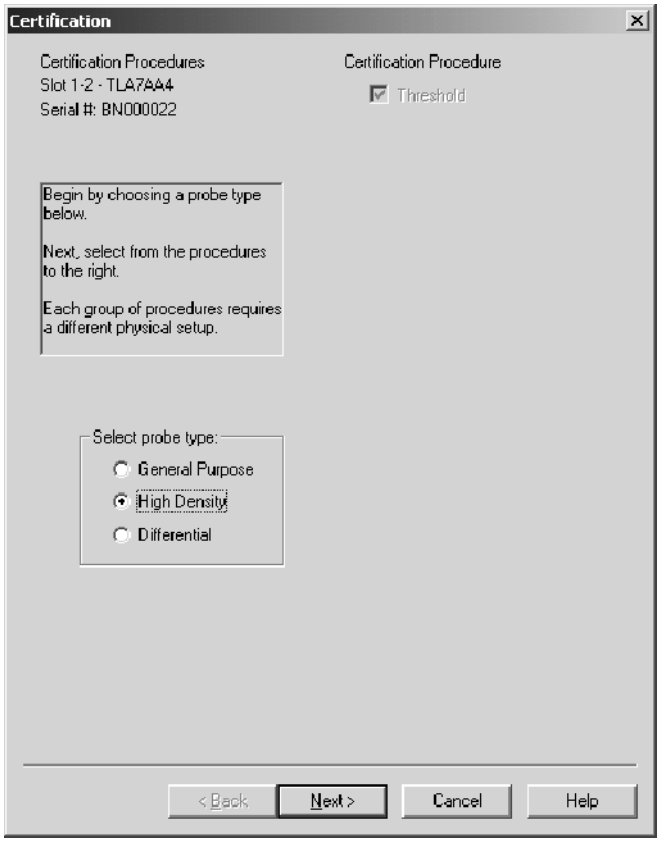


**Figure 4-7: Default Certification procedure dialog box**

8. After the first set of procedures are done, click the Next button to display the instructions for the next step. In most cases you only need to connect a different probe to the test fixture.
9. After changing the connections, click the Next button to continue the tests.
10. Repeat steps 8 through 9 as indicated by the software.
11. After the procedure finishes, click the Next button to open the Finish dialog box where you can save the results to a file. Enter a file name and click the Save button. You can use the Save dialog to save the file to a folder of your choice or use the default location.
12. Click the Finish button to complete the process.
13. Locate the file that you saved in step 11 and print the file for your records.

***CAUTION.*** *Always disconnect one end of each P6041 cable before powering down the TLACAL2 test fixture. Failure to do so can damage the test fixture.*

**14.** Disconnect one end of each P6041 cable before powering down the TLACAL2 test fixture.

**15.** Power down the TLACAL2 test fixture and then disconnect the remaining test equipment.

This completes the certification procedures.

# Adjustment Procedures

This chapter contains procedures which use the performance verification software to adjust the logic analyzer modules to within factory specifications. The software contains instructions and control programs for adjusting the logic analyzer. The software describes test equipment connections and settings, selects setup parameters, and loads calibration constants into memory.

***NOTE**. There are no adjustment procedures for the TLACAL2 Performance Verification test fixture in this section. If the test fixture requires any adjustments, you must return the test fixture to the factory; contact your local Tektronix service center for more information.*

These procedures adjust the logic analyzer module for conformance with the warranted characteristics listed in the *Specifications* chapter of this manual.

Perform the adjustments after repairing the module or when performance verification tests have failed.

## Test Equipment and Initial Setup

The adjustment procedures use the same test equipment and setups as listed in the Performance Verifications chapter. Refer to those sections for additional information before starting the adjustment procedures.

## Prerequisites

***NOTE**. The performance verification software reads the serial number of the logic analyzer module from information stored in the LPU board. If you have replaced the LPU board, verify that the serial number on the label of the module matches the serial number read by the software before beginning the adjustment procedures.*

Perform these procedures after meeting the following requirements:

- The logic analyzer application must not be running.
- The performance verification software must be installed on the hard disk of the logic analyzer mainframe. Refer to *Software Installation* on page 2–7 for more information.
- The logic analyzer module must be installed in a Tektronix logic analyzer mainframe.
- The logic analyzer, TLACAL2 fixture, and all other test equipment require a 30-minute warm-up time in a +20 °C to +30 °C environment before performing any adjustments. Adjustments performed before the operating temperature has stabilized may cause errors in performance.
- The logic analyzer and TLACAL2 test fixture must be in an operating environment within the limits described in the *Specifications* chapter of this manual.
- If you are using P6860 probes or P6880 probes, you must use the thick board elastomers (available in the 020-2452-xx accessory kit). Refer to the *Operating Basics* chapter of the *P6810, P6860, & P6880 Logic Analyzer Probe Instruction Manual* for instructions on installing or changing the elastomers.

## Merged Modules

The performance verification software runs independent of the logic analyzer application but it recognizes configuration settings. It is not necessary to unmerge modules before performing the adjustment procedures on merged modules.

When adjusting merged modules using different types of individual modules, the adjustment procedure can be done on the merged module without physical separation.

## Using the Software

This section describes how to perform adjustments using the software.

### Performing the Adjustments

There are no manual adjustments for the logic analyzer modules. The software adjusts the instrument hardware using external test equipment connections that you provide in response to prompts on the screen.

Upon successful completion of each adjustment, the software automatically loads the new calibration data into memory.

### Adjustment After Repair

You must perform all adjustment procedures following replacement of any circuit board in the logic analyzer module.

This section describes how to perform adjustments using the software.

## Tests Performed

Table 5–1 lists the adjustment procedures available for the logic analyzer module and for the related probes.

**Table 5-1: Logic analyzer adjustment procedures**

| Category | Procedure |
|---|---|
| Self calibration | Self Calibration |
| Probe+PIC Procedures | Probe Gain and Offset |
| Module+MIC Procedures | Input Resistance<br>Digital Gain and Offset<br>Analog Gain and Offset |
| Probe+Module Timing Procedures | Deskew |
| Merged Deskew Procedures | Merged Deskew |

With the exception of the self calibration procedures, all other procedures must be completed using the performance verification software and the TLACAL2 test fixture.

The Probe+PIC Procedure is an optional procedure used to calibrate the probe gain and offset settings; you should not normally need to perform this procedure. The probes are calibrated at the factory. However the procedure is provided so that you can do a full calibration of your logic analyzer and probes if needed.

The Merged Deskew procedures are recommended for merged module configurations.

Figure 5–1 shows the locations of connectors and test points on the TLACAL2 Performance Verification test fixture. You may need to refer to this illustration when connecting probes and cables to the fixture.

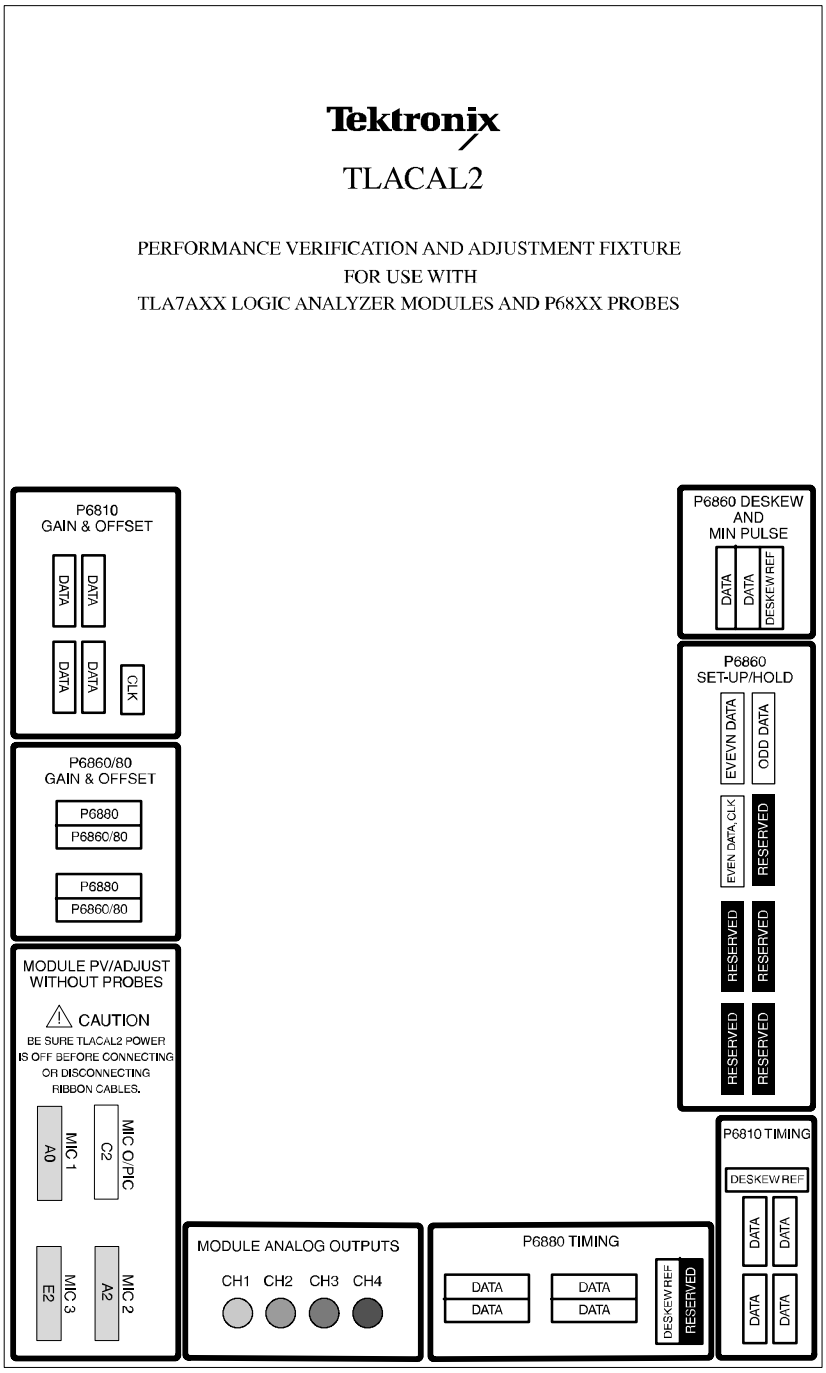


**Figure 5- 1: TLACAL2 test fixture connections**

## Self Calibration

Self calibration is an internal routine that optimizes performance at the current ambient temperature to maximize measurement accuracy. No external equipment or user actions are needed to complete the procedure. The logic analyzer module saves data generated by the self calibration in nonvolatile memory. Passing self cal provides a higher level of confidence of module functionality.

***NOTE**. Performing the self calibration does not guarantee that all parameters operate within limits. Operation within limits is achieved by performing the adjustment procedures. Verification of operation within limits is accomplished by performing the performance verification procedures.*

You can run the self calibration at any time during normal operation. To maintain measurement accuracy, perform the self calibration if the following conditions occur:

- After repair and replacement of any circuit board.
- It has been a year since the last self calibration was run.

1. Ensure that the instrument has had a 30-minute warm up before attempting the self calibration, and that the logic analyzer application is running.
2. Disconnect any probes connected to the logic analyzer module.
3. Select Calibration and Diagnostics from the System menu.
4. Select the Self Calibration tab page.
5. Select the logic analyzer module.
6. Click the Run button to start the self calibration.

   The self calibration takes several minutes to complete, depending on the number of channels in the module. Upon successfully completing the self calibration, the module status changes from Running to Calibrated, and the Date and Time field is set to the present.

# Probe+PIC Procedures

The Probe+PIC Procedures consist of the Probe Gain and Offset procedures for the P6810, P6860, and P6880 logic analyzer probes. These procedures are optional and are not required to adjust the logic analyzer module. The probes are adjusted at the factory before shipment and should not require readjustment.

The following procedure assumes that you will be adjusting one probe at a time without performing any other module adjustments.

## Equipment Setups

These procedures require the same setups as described in the Performance Verification chapter of this manual. It is assumed that the logic analyzer mainframe is already connected to the TLACAL2 test fixture and that the performance verification software is installed on the hard disk of the logic analyzer. The following procedures describe the specific connections from the probes to the TLACAL2 test fixture.

***CAUTION.*** *Always power down the TLACAL2 test fixture before connecting or disconnecting the ribbon cables. Failure to do so can damage the test fixture, the PIC, or the MICs.*

1. Power down the TLACAL2 test fixture before connecting the ribbon cables and the PIC.

***CAUTION.*** *To avoid damaging the test fixture and the PIC through static discharge, always wear a grounded antistatic wrist strap. Avoid handling individual components of the test fixture without static protection.*

2. Connect one of the ribbon cables to the MIC0/PIC connector (J141) on the test fixture.
3. Connect the PIC to the other end of the ribbon cable.
4. Connect any one of the coaxial cables from the TV (test voltage) connectors on the test fixture to the TV connector on the PIC.
5. Connect the multimeter leads to the DMM test points (J390) on the test fixture. Connect the positive lead to the + connector and the negative (ground) lead to the – connector.
6. Connect the probe to be adjusted to the PIC.
7. If you are adjusting a P6810 probe:
   a. Connect the lead sets to the P6810 GAIN & OFFSET Data connections at J100, J101, J110, and J111 on the test fixture.

**b.** Connect the clock/qualifier leads to the SNGL square pins at J220. Make sure that you connect the ground side or the "–" side to the square pins with the GND label. There is no need to connect the single ground wire.

**8.** If you are adjusting a P6860, connect the probe heads to the P6860/80 GAIN & OFFSET connections at J120 and J130 on the test fixture. If you have a P6880 probe, connect the probe heads to J120, J121, J130, and J131 on the test fixture.

**9.** Power on the test fixture, logic analyzer, and digital multimeter and allow all test equipment to warm up for 30 minutes before continuing the adjustments.

## Start the Software

Complete the following steps to start the performance verification software and to run the adjustments:

**1.** Exit the TLA application on the logic analyzer.

**2.** Double-click the TLA7Axx Performance Verification icon on the desktop. An application window similar to Figure 5–2 appears.


**Figure 5-2: Performance verification software startup window**

**3.** Click the Adjustment button to start the software. An Adjustment Procedure dialog box similar to Figure 5–3 appears.

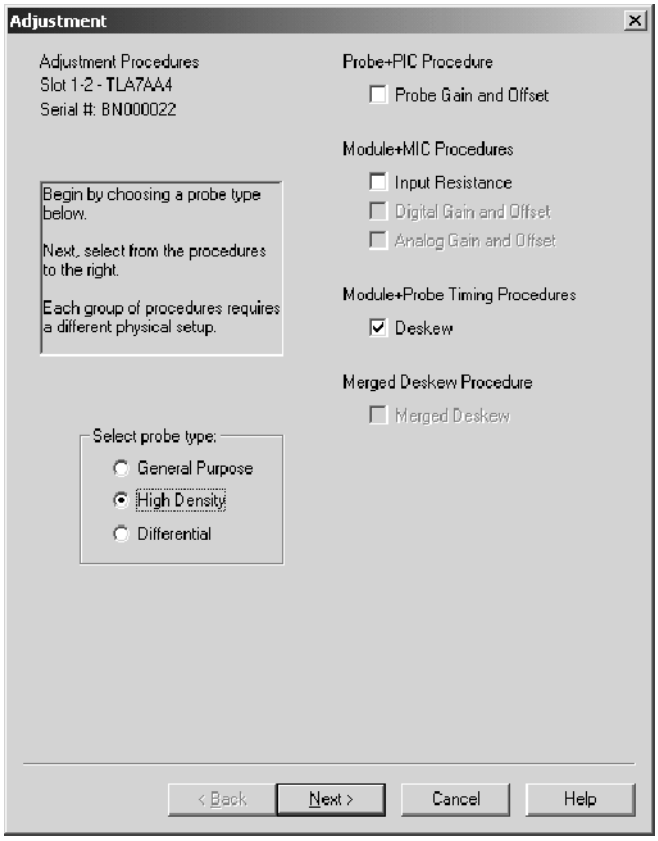


**Figure 5-3: Default Adjustment procedure dialog box**

4. Select the probe type near the bottom of the dialog box.
5. Select the Probe Gain & Offset procedure (the default selection is not selected); clear any other procedures.

***NOTE**. The software will perform all selected procedures in the listed sequence. To limit the test to specific procedures, clear any procedures that you do not want to run.*

6. Click the Next button at the bottom of the dialog box to begin the adjustment procedure.

   A list of connection instructions displays for the current procedure.

7. Verify that your connections match those of the instructions. Then click the Next button to begin the adjustment procedures.

   The software will begin the adjustment procedures and display a list of results in the window.

8. After the procedure finishes, click the Next button to open the Finish dialog box where you can save the results to a file. Enter a file name and click the Save button. You can use the Save dialog to save the file to a folder of your choice or use the default location.
9. If you are adjusting more than one probe, disconnect the first probe and connect the next probe. There is no need to power down the test fixture while changing probes.
10. Click the Back button to return to the instructions dialog.
11. Click the Next button to restart the procedure.
12. After completing the adjustments on the last probe, you can exit the application or return to the main window to perform other procedures.

***CAUTION.*** *Power down the test fixture before disconnecting the PIC from the test fixture. Failure to do so can damage the test fixture or the PIC.*

## Module+MIC Procedures

The Module+MIC Procedures consist of the Input Resistance adjustments, the Digital Gain and Offset adjustments, and the Analog Gain and Offset adjustment procedures for the logic analyzer modules. These procedures are required to adjust the logic analyzer module. These procedures use the module interface connectors (MICs), the TLACAL2 test fixture and accessories, and the software. No logic analyzer probes are required to complete these adjustments.

### Equipment Setups

These procedures require the same setups as described in the Performance Verification chapter of this manual. It is assumed that the logic analyzer is already connected to the TLACAL2 test fixture and that the performance verification software is installed on the hard disk of the logic analyzer. It is also assumed that the logic analyzer module is installed in the logic analyzer mainframe. The following procedures describe the specific connections from the logic analyzer module to the probes and to the TLACAL2 test fixture.

***CAUTION.*** *If you have any P6041cables connected from the logic analyzer to the TLACAL2 test fixture, always disconnect one end of each P6041 cable before powering down the test fixture.*

*Always power down the test fixture before connecting or disconnecting ribbon cables. Failure to do so can damage the test fixture, the PIC, or the MICs.*

1. Power down the TLACAL2 test fixture before connecting the ribbon cables and the MICs.

***CAUTION.*** *To avoid damaging the test fixture and the PIC through static discharge, always wear a grounded antistatic wrist strap. Avoid handling individual components of the test fixture without static protection.*

2. Connect the four ribbon cables to the ribbon cable connectors on the test fixture.
3. Disconnect the PIC if it is connected to the ribbon cable.
4. Connect a MIC to each of the ribbon cables.
5. Connect any one of the coaxial cables from the CS (current source) connectors on the test fixture to the CS connector on the MIC.
6. Connect any one of the coaxial cables from the TV (test voltage) connectors on the test fixture to the TV connector on the MIC.
7. Connect the multimeter leads to the DMM test points (J390) on the test fixture. Connect the positive lead to the + connector and the negative (ground) lead to the – connector.
8. Connect a P6041 cable from each of the Analog Output BNC connectors to the corresponding connector on the front of the test fixture (if necessary, refer to the label on the test fixture for the connection locations).
9. Connect the ribbon cables with the MICs to the appropriate connector on the logic analyzer module.
10. Power on the test fixture and allow for a 30 minute warmup.

## Start the Software

Complete the following steps to start the software and to run the adjustments:

1. Exit the TLA application on the logic analyzer.
2. Double-click the TLA7Axx Performance Verification icon on the desktop. An application window similar to Figure 5–2 on page 5–7 appears.
3. If you have more than one logic analyzer module in your mainframe, select the logic analyzer module from the list in the window.
4. Click the Adjustment button to start the software. An Adjustment dialog box similar to Figure 5–3 on page 5–8 appears.
5. Select the Input Resistance procedure and clear any other procedures.

***NOTE**. The software will perform all selected procedures in the listed sequence. To limit the test to specific procedures, clear any procedures that you do not want to run.*

*If you leave the Deskew procedure selected, you will be prompted to move the probe connections before you continue the procedure. This procedure assumes that you clear the Deskew procedure.*

6. Click the Next button at the bottom of the dialog box to begin the procedure.

   A list of connection instructions displays.

7. Verify that your connections match those of the instructions. Then click the Next button to begin the procedures.

   The software will begin the adjustment procedures and display a list of test results in the window.

8. After the procedure finishes, click the Next button to open the Finish dialog box where you can save the results to a file. Enter a file name and click the Save button. You can use the Save dialog to save the file to a folder of your choice or use the default location.

9. Click the Finish button to finish the next procedure and return to the startup window.

# Module+Probe Timing Procedures

The Module+Probe Timing procedures consist of the deskew adjustments. These procedures are required to adjust the logic analyzer module. These procedures use the logic analyzer probes connected to the Deskew and Minimum Pulse connections on the TLACAL2 test fixture. Depending on the type of probe that you are using and on the number of channels of your logic analyzer module, the test connections differ.

## Equipment Setups

These procedures require the same setups as described in the Performance Verification chapter of this manual. It is assumed that the logic analyzer is already connected to the test fixture and that the performance verification software is installed on the hard disk of the logic analyzer. It is also assumed that the logic analyzer module is installed in the logic analyzer mainframe. The following procedures describe the specific connections from the logic analyzer module to the probes and the TLACAL2 test fixture.

***CAUTION.*** *Always disconnect one end of each P6041 cable before powering down the TLACAL2 test fixture. Failure to do so can damage the test fixture.*

1. If connected, remove the P6041 cable from the Analog Output BNC connectors and from the test fixture.

***CAUTION.*** *Always power down the TLACAL2 test fixture before connecting or disconnecting the ribbon cables. Failure to do so can damage the test fixture, the PIC, or the MICs.*

2. Disconnect the MICs and ribbon cables from the logic analyzer module.

***NOTE****. Depending on your logic analyzer module, you can use only one logic analyzer probe to complete these procedures and move the probes between the module input connectors as indicated by the software instructions. However to obtain the best results, you should keep the probes connected to the logic analyzer module and only move the connections on the test fixture.*

3. Connect a probe to each probe connector on the logic analyzer module.
4. Refer to Table 5–2 on page 5–13 and to Figure 5–4 on page 5–14 to connect the probe from the logic analyzer C0/C1/C2/C3 input connector (or the C3/C2/A3/A2 connector if you have a 34- or 68-channel module) to the appropriate connectors on the test fixture.

***NOTE**. Make sure that the alignment pin on the P6860 or P6880 probe head is aligned with the hole on the test fixture. Tighten the probe head screws by alternating between them until they are finger tight (no more than 1 in-lbs of torque).*

5. If you are using a P6810 probe, make sure that you connect the ground or low side of the lead sets to the GND side of the connectors on the test fixture. Connect the clock/qualifier leads to the DESKEW REF connector; make sure that you connect the ground side or the "–" side to the square pins with the GND label. The single ground wire does not need to be connected.

6. Power on the test fixture and allow it to warm up for 30 minutes before continuing the the adjustment procedures.

**Table 5-2: Deskew procedure probe connections**

| Probe | TLACAL2 connections |
|---|---|
| P6810 | P6810 TIMING<br>(J881, J882, J883, J884 data connectors<br>J880 Deskew Ref connector) |
| P6860 | P6860 DESKEW AND MIN PULSE<br>(J610, J611 data connectors<br>J612 deskew ref connector) |
| P6880 | P6880 TIMING<br>(J581, J582, J583, J584 data connectors,<br>J680 Deskew Ref connector) |

## Start the Software

Complete the following steps to start the software and to run the adjustments:

1. Exit the TLA application on the logic analyzer.

2. Double-click the TLA7Axx Performance Verification icon on the desktop. An application window similar to Figure 5–2 on page 5–7 appears.

3. If you have more than one logic analyzer module in your mainframe, select the logic analyzer module to be adjusted from the list in the window.

4. Click the Adjustment button to start the software. An Adjustment dialog box similar to Figure 5–3 on page 5–8 appears.

5. Select Deskew under the Module+Probe Timing Procedures and clear any other procedures.

***NOTE**. The software will perform all selected procedures in the listed sequence. To limit the test to specific procedures, clear any procedures that you do not want to run.*

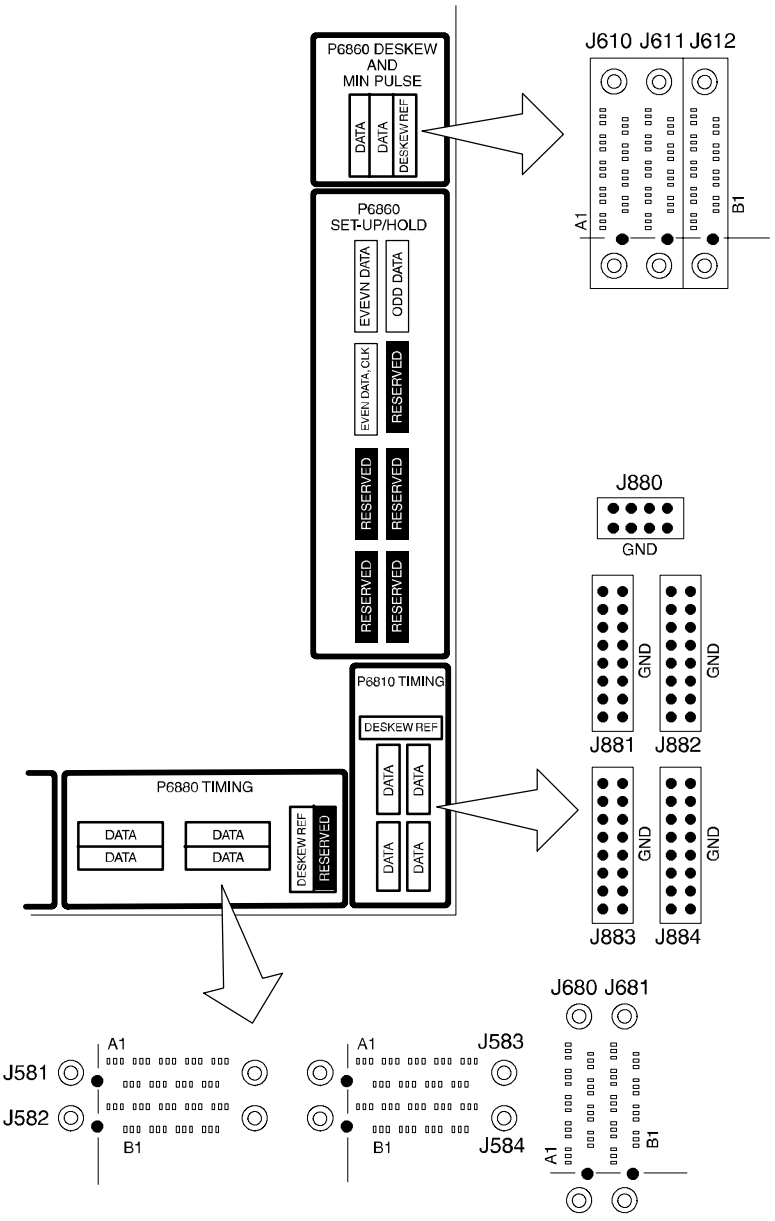


**Figure 5- 4: Deskew procedure probe connections**

6. Click the Next button at the bottom of the dialog box to begin the adjustment procedure.

   A list of connection instructions displays for the current procedure.

7. Verify that your connections match those of the instructions. If you are using P6860 or P6880 probes, make sure that the alignment pin on the P6860 or P6880 probe head aligns with the hole in the test fixture. Tighten the probe head screws by alternating between them until they are finger tight (no more than 1 in-lbs of torque). If you are using P6810 probes, there is no need to connect the single ground wire.

8. Click the Next button to begin the procedures.

   The software will begin the adjustment procedures and display the results of the first 34 channels in the window.

---

***NOTE**. If any failures occur, you must complete the entire test sequence. Do not click the Back button; otherwise the test results will be incorrect. Address the problem and then restart the Deskew procedures.*

---

9. Click the Next button.

10. If you have a 34-channel module, go to step 15. If your module has more than 34 channels, connect the next probe as indicated by the software instructions.

11. If you are using P6860 or P6880 probes, move the CK3 probe head to the appropriate DESKEW REF connection on the test fixture. Leave the probe head connected for the remainder of the procedure. If you are using P6810 probes, disconnect the lead sets from the DATA connector, but leave the CK3 connection on the DESKEW REF (J880) connector.

12. Connect the next probe to the appropriate DATA connects on the test fixture. For P6810 probes, connect the data leads to the Data connector and the clock/qualifier leads to the DESKEW REF connector.

13. Click the Next button to start testing the next probe input section.

14. Repeat steps 12 and 13 for the remaining probe channel sections. Do not move the CK3 probe head or the CK3 lead connected to the DESKEW REF connector.

15. Click the Next button to save the deskew adjustment values.

16. After the procedure finishes, click the Next button to open the Finish dialog box where you can save the results to a file. Enter a file name and click the Save button. You can use the Save dialog to save the file to a folder of your choice or use the default location.

17. Click the Finish button to finish the procedure and return to the startup window.

## Merged Deskew Procedures

The Merged Deskew procedures adjusts the deskew between modules in a merged module set. These procedures use the logic analyzer probes connected to the Deskew and Minimum Pulse connections on the TLACAL2 test fixture. Depending on the type of probe that you are using and on the number of channels of your logic analyzer module, the test connections differ. You should run these procedures after you have completed the individual module merge procedure.

### Equipment Setups

These procedures require similar setups as described in the Performance Verification chapter of this manual. It is assumed that the logic analyzer is already connected to the test fixture and that the performance verification software is already installed on the hard disk of the logic analyzer. It is also assumed that the logic analyzer modules are installed in the logic analyzer mainframe. The following procedures describe the specific connections from the logic analyzer modules to the probes and the TLACAL2 test fixture.

These procedures adjust one pair of modules at a time. When connecting the probes to the modules, make sure that you know which module is the master module and which module is the slave module.

1. Connect a probe from the C0/C1/C2/C3 input connector (or the C3/C2/A3/A2 connector) on the slave module to the appropriate DATA connector as listed in Table 5–3.

2. Connect a probe from the C0/C1/C2/C3 input connector (or the C3/C2/A3/A2 connector) on the master module to the appropriate DESKEW REF connector as listed in Table 5–3.

---

***NOTE**. If you are using P6860 probes or P6880 probes, make sure that the alignment pin on the probe head is aligned with the hole on the test fixture. Tighten the probe head screws by alternating between them until they are finger tight (no more than 1 in-lbs of torque).*

---

3. If you are using a P6810 probe, make sure that you connect the ground or low side of the lead sets to the GND side of the connectors on the test fixture. Connect the clock/qualifier leads to the DESKEW REF (J880) connector; make sure that you connect the ground side or the "–" side to the square pins with the GND label. There is no need to connect the single ground wire.

4. Power on the test fixture and allow it to warm up for 30 minutes before continuing the the adjustment procedures.

**Table 5-3: Merged Deskew procedure probe connections**

| Probe | TLACAL2 connections |
|---|---|
| P6810 | P6810 TIMING<br>(J881, J882, J883, J884 data connectors<br>J880 Deskew Ref connector) |
| P6860 | P6860 DESKEW AND MIN PULSE<br>(J610, J611 data connectors<br>J612 deskew ref connector) |
| P6880 | P6880 TIMING<br>(J581, J582, J583, J584 data connectors,<br>J680 Deskew Ref connector) |

## Start the Software

Complete the following steps to start the software and to run the adjustments:

1. Exit the TLA application on the logic analyzer.
2. Double-click the TLA7Axx Performance Verification icon on the desktop. An application window similar to Figure 5–2 on page 5–7 appears.
3. If you have more than one logic analyzer module in your mainframe, select the logic analyzer module to be adjusted from the list in the window.
4. Click the Adjustment button to start the software. An Adjustment dialog box similar to Figure 5–3 on page 5–8 appears.
5. Select Merged Deskew under the Merged Deskew Procedures and clear any other procedures.

***NOTE**. The software will perform all selected procedures in the listed sequence. To limit the test to specific procedures, clear any procedures that you do not want to run.*

6. Click the Next button at the bottom of the dialog box to begin the adjustment procedure.

   A list of connection instructions displays for the current procedure.

7. Verify that your connections match those of the instructions. Then click the Next button to begin the procedures.

   The software will begin the adjustment procedures and display a list of results in the window.

8. After the procedure finishes, click the Next button to open the Finish dialog box where you can save the results to a file. Enter a file name and click the Save button. You can use the Save dialog to save the file to a folder of your choice or use the default location.

9. Click the Finish button to finish the next procedure and return to the startup window.

## Completing the Adjustment Steps

After completing the adjustment procedures, you should always run the *Performance Verification Procedures* to verify that the all parameters are within the allowable specifications. If any of the adjustment and performance verification procedures fail, further service may be necessary. Contact your local Tektronix service center for recommended action.

# Maintenance

This chapter contains the information needed for periodic and corrective maintenance of the Logic Analyzer Modules. The following sections are included.

- This *Maintenance* section provides general information on preventing damage to internal circuit boards when doing maintenance, procedures for inspecting the logic analyzer module, and cleaning external and internal circuit boards.
- The *Removal and Installation Procedures* (page 6–9) provide procedures for removing and installing circuit boards and other common replaceable parts.
- *Troubleshooting* (page 6–25) provides information for isolating faulty circuit boards, probes, and other faults.
- *Repackaging Instructions* (page 6–39) provides packaging information for shipment or storage.

## Related Maintenance Procedures

The *TLA7UP Mainframe Field Upgrade Instruction Manual* contains some maintenance procedures not included in this manual. Refer to the *TLA7UP Mainframe Field Upgrade Instruction Manual* for information on upgrading the mainframe software or module firmware.

## Preventing Electrostatic Discharge

When performing any service that requires internal access to the logic analyzer module, adhere to the following precautions to avoid damaging internal modules and their components due to electrostatic discharge (ESD).

***CAUTION.*** *Static discharge can damage any semiconductor component.*

- Minimize handling of static-sensitive modules.
- Transport and store static-sensitive modules in their static protected containers. Label any package that contains static-sensitive modules.
- Wear a grounded antistatic wrist strap while handling these modules. Service static-sensitive modules only at a static-free work station.

- Nothing capable of generating or holding a static charge should be allowed on the work surface.
- Handle circuit boards by the edges when possible.
- Do not slide the modules over any surface.
- Avoid handling the modules in areas that have a floor or work surface capable of generating a static charge.

## Inspection and Cleaning

Inspection and cleaning are done as preventive maintenance. Preventive maintenance, when done regularly, may prevent malfunctions and enhance reliability.

Preventive maintenance consists of visually inspecting and cleaning the instrument, and using general care when operating it. How often to perform maintenance depends on the severity of the environment in which the instrument is used. A proper time to perform preventive maintenance is just before performing performance verification procedures or as an incoming inspection.

### General Care

The side cover keeps dust out of the instrument and should be in place during normal operation.

### Inspection and Cleaning Procedures

Inspect and clean the instrument as often as operating conditions require. Collection of dirt on internal components can cause them to overheat and breakdown. Dirt acts as an insulating blanket, preventing efficient heat dissipation. Dirt also provides an electrical conduction path that can cause failures, especially under high-humidity conditions.

***CAUTION.*** *Avoid using chemical cleaning agents that might damage the plastics and external labels used in the instrument.*

*Use a cloth dampened with water to clean external surfaces. To prevent damage to electrical components from moisture during external cleaning, use only enough liquid to dampen the cloth or applicator.*

*Use a 75% isopropyl alcohol solution to clean internal surfaces and rinse with deionized water. Before using any other type of cleaner, consult your Tektronix Service Center or representative.*

## Exterior Inspection

Inspect the outside of the instrument for damage, wear, and missing parts. Use Table 6–1 as a guide. Instruments that appear to have been dropped or otherwise abused should be checked thoroughly to verify correct operation and performance.

Immediately repair defects that can cause personal injury or lead to further damage to the logic analyzer module or mainframe where it is used.

**Table 6-1: External inspection check list**

| Item | Inspect for | Repair action |
|---|---|---|
| Front panel and side cover | Cracks, scratches, deformations, missing or damaged retainer screws, ejector handles, or EMI shields. | Replace defective or missing mechanical parts. |
| Front panel connectors | Broken shells, cracked insulation, and deformed contacts.<br>Dirt in connectors. | Replace defective parts or clean parts based on the cleaning procedures. |
| Rear connectors | Cracked or broken shells, damaged or missing contacts.<br>Dirt in connectors. | Replace defective parts or clean parts based on the cleaning procedures. |
| Accessories | Missing items or parts of items, bent pins, broken or frayed cables, and damaged connectors. | Replace damaged or missing items, frayed cables, and defective modules. |

## Exterior Cleaning Procedure

To clean the exterior, perform the following steps:

1. Remove loose dust on the outside of the logic analyzer module with a lint free cloth.
2. Remove remaining dirt with a lint-free cloth or applicator and water, using only enough liquid to dampen the cloth or applicator. Do not use abrasive cleaners.

## Interior Inspection

Inspect the internal portions of the logic analyzer module for damage and wear using Table 6–2 as a guide. When found, defects should be repaired immediately. If you must replace an internal component, refer to the *Removal and Installation Procedures*, later in this chapter, for detailed removal and replacement instructions.

***CAUTION.*** *Do not attempt to repair any circuit boards with a soldering iron. Most of the internal components are surface mounted devices. Using a soldering iron can damage the surface-mounted components and internal circuit boards. Refer the replacement of surface-mounted components to qualified service personnel with the appropriate tools.*

**Table 6-2: Internal inspection check list**

| Item | Inspect for | Repair action |
|---|---|---|
| Circuit boards | Loose, broken, or corroded connections. Burned circuit boards. Burned, broken, or cracked circuit-run plating. | Remove failed circuit board and replace with a new one. |
| Resistors | Burned, cracked, broken, blistered condition. | Remove failed circuit board and replace with a new one. |
| Capacitors | Damaged or leaking cases. Corroded solder on leads or terminals. | Remove failed circuit board and replace with a new one. |
| Semiconductors | Damaged parts or distorted pins. | Replace circuit board if parts are damaged. |
| Wiring and cables | Loose plugs or connectors. Burned, broken, or frayed wiring. | Firmly seat connectors. Repair or replace circuit boards with defective wires or cables. |

***CAUTION.*** *To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the logic analyzer module.*

## Interior Cleaning Procedure

To clean the interior, perform the following steps:

1. Blow off dust with dry, low-pressure, deionized air (approximately 9 psi).
2. Remove any remaining dust with a lint free cloth dampened in isopropyl alcohol (75% solution) and rinse with warm deionized water. (A cotton-tipped applicator is useful for cleaning in narrow spaces and on circuit boards.)

***NOTE**. If, after performing steps 1 and 2, a module is clean upon inspection, skip the remaining steps. If steps 1 and 2 do not remove all the dust or dirt, the module may be spray washed using a solution of 75% isopropyl alcohol (see steps 3 through 7).*

3. Gain access to the parts to be cleaned by removing easily accessible shields and panels (see *Removal and Installation Procedures* on page 6–9).
4. Spray wash dirty parts with the isopropyl alcohol and wait 60 seconds for the majority of the alcohol to evaporate.
5. Use warm (48.9 °C to 60 °C / 120 °F to 140 °F) deionized water to thoroughly rinse the parts.
6. Dry all parts with low-pressure, deionized air.
7. Dry all components and assemblies in an oven or drying compartment using low-temperature (51.7 °C to 65.6 °C / 125 °F to 150 °F) circulating air.

## Cleaning the Probes

To clean the exterior surfaces of the probes, remove dirt and dust with a soft brush. For more extensive cleaning, use only a damp cloth. Never use abrasive cleaners or organic solvents

***CAUTION.** Static discharge can damage any semiconductor component in the probe head. Always wear a grounded antistatic wrist strap whenever handling the probe head. Also verify that anything to which the probe head is connected does not carry a static charge.*

***NOTE**. Never clean the elastomers. Always replace them instead. Refer to the* P6810, P6860, P6880 Logic Analyzer Probe Instruction Manual *for information on replacing the probe elastomers and other probe accessories.*

The P6860 and P6880 probes require special cleaning attention. Clean the probe heads according to the following steps:

1. Moisten a cotton swab with isopropyl alcohol.
2. Gently wipe the edge print pads of the hybrid.
3. Remove any remaining lint using a nitrogen air gun.

## Cleaning the P6860 and P6880 Compression Footprints

***CAUTION.*** *To avoid electrical damage, always turn off the power of your target system before cleaning the compression footprint.*

Prior to connecting the probe to the target system, the compression footprints on the target system must be properly cleaned. Clean the compression footprints according to the following steps:

1. Use a lint-free cloth moistened with isopropyl alcohol and gently wipe the footprint surface.
2. Remove any remaining lint using a nitrogen air gun.

***NOTE****. Use alcohol sparingly and be sure that you have removed any remaining lint or residue with the nitrogen air gun.*

## Cleaning the P6860 and P6880 Probe Heads

Before connecting the P6860 and P6880 Probes to the target system, ensure that the probe heads are free from dust, dirt, and contaminants. If necessary, clean the probe heads according to the following steps.

***CAUTION.*** *Static discharge can damage semiconductor components in the probe head. Always wear a grounded antistatic wrist strap whenever handling the probe head. Also verify that anything to which the probe head is connected does not carry a static charge.*

***NOTE****. Never clean the elastomers. Always replace them instead. Refer to the* Operating Basics *chapter of the* P6810, P6860, & P6880 Logic Analyzer Probe Instruction Manual *for information on replacing elastomers.*

1. Remove elastomer holder (see Figure 6–1).
2. Moisten a cotton swab with isopropyl alcohol.

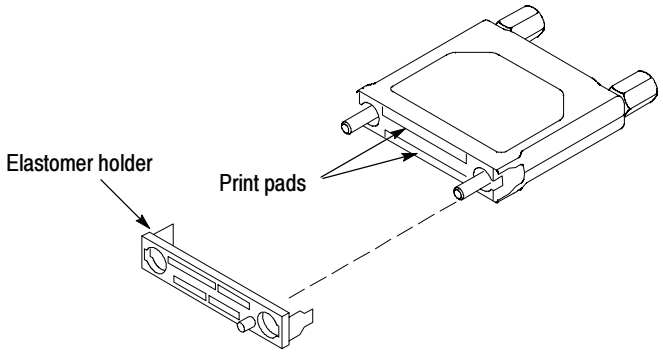


**Figure 6-1: Cleaning the probe heads**

3. Gently wipe the edge print pads of the hybrid.
4. Remove any remaining lint using a nitrogen air gun.
5. Put the elastomer holder back in place.

***CAUTION.*** *Do not touch the elastomers to avoid damaging the probe contacts.*

## Storing the P6860 and P6880 Probe Heads

To protect the elastomer, it is important to properly store the probe heads when the probes are not in use. See Figure 6-2.

1. Locate the keying pin on the probe end and align it to the keying pin hole on the nutbar.
2. While holding the probe end at a perpendicular angle to the nutbar, finger-tighten both probe head screws until snug (no more than 1 in-lbs of torque).

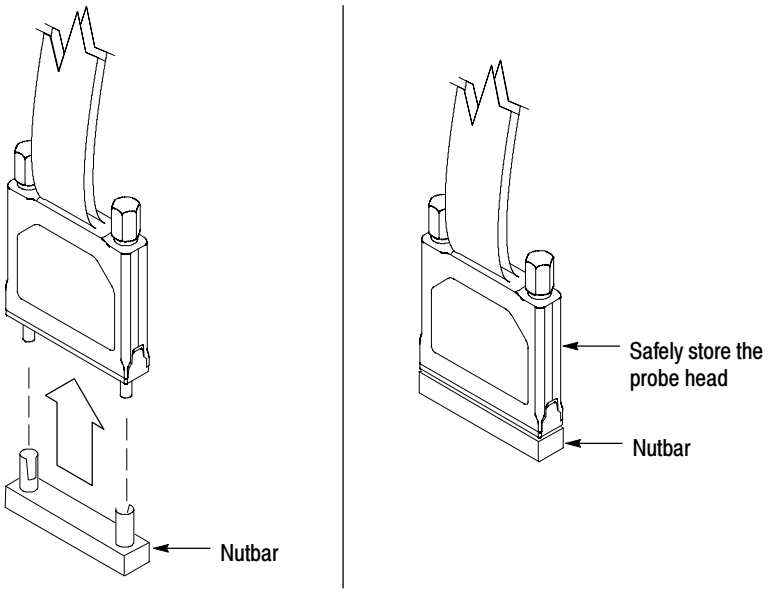


**Figure 6- 2: Storing the probe head**

# Removal and Installation Procedures

This section describes how to remove and install the major mechanical and electrical modules. The procedures in this section assume that you already have removed the module from the mainframe.

***WARNING.*** *Before doing any procedures in this manual, read the* General Safety Summary *and* Service Safety Summary *found at the beginning of this manual.*

*To prevent possible injury to service personnel or damage to electrical components, read* Preventing Electrostatic Discharge *on page 6–1.*

## Tools Required

Table 6–3 lists the tools needed to replace the internal components of the logic analyzer module.

**Table 6-3: Tools required for circuit board replacement**

| Name | Description |
|---|---|
| Screwdriver with a T-9 and a T-10 Torx tip | Standard tool |
| 1/4-inch nut driver | Standard tool |
| 9/16-inch nut driver | Standard tool |
| Needle-nose pliers | Standard tool |

## Torque Requirements

Tighten all T-9 and T-10 screws to 4 in. lbs. Tighten standoff posts to 8 in. lbs.

# Injector/Ejector Handles

You will need a screwdriver with a T-10 tip to complete the following procedures.

## Removal

Use the following procedure to remove the injector/ejector handles:

1. Place the module on the right side (see Figure 6–3).
2. Remove the two screws that secure the injector/ejector handle to the chassis.
3. Remove the injector/ejector handle from the module.

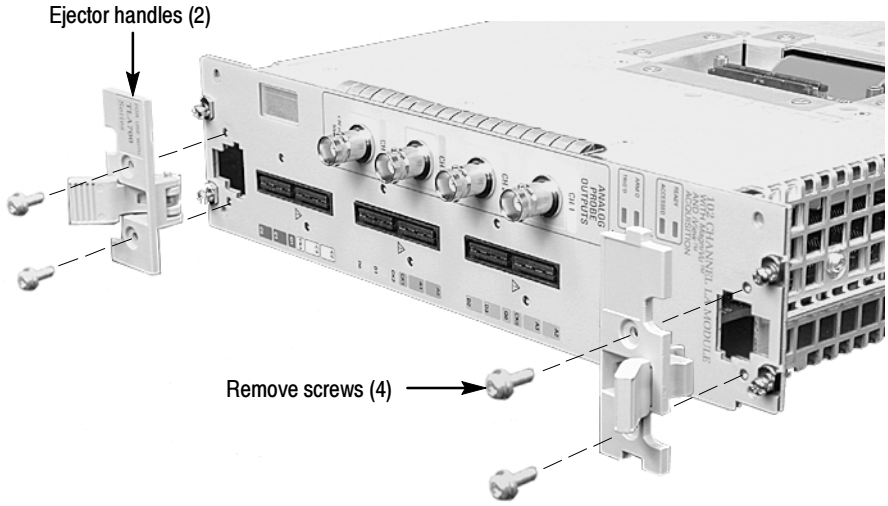


**Figure 6- 3: Injector/ejector handle replacement**

### Installation

Use the following procedure and Figure 6–3 to install the injector/ejector handles:

***NOTE**. The top and bottom injector/ejector handles are not interchangeable. The top injector/ejector handle assembly has a notch on right side and a tab on the left side; the bottom injector/ejector handle assembly does not have a notch or a tab.*

1. Install the injector/ejector handle through the front panel cutout onto the mounting post.
2. Install the screws to secure the injector/ejector handle to the chassis.
3. Apply the proper replacement label (see the *Replaceable Mechanical Parts List* for label part numbers if necessary).

## Covers

You will need a screwdriver with a T-9 and a T-10 tip to complete the following procedures.

### Removal

Use the following procedure and Figures 6–4 and 6–5 to remove the covers:

1. Place the module on the right side.
2. Remove the two screws on the rear of the chassis and the two rear screws, located on either side of the rear panel, that secure the rear panel to the chassis.
3. Remove the rear panel and set it aside.
4. Remove the two top screws and the two bottom screws that secure the cover to the chassis.
5. If you have a 102-channel module or a 136-channel module with a merge cable, complete to following steps (refer to Figure 6–4 as necessary):
   a. Remove the eight T-9 countersunk screws holding the bracket to the cover.
   b. Lift the assembly out of the cover and then reach into the hole and disconnect the merge cable from the circuit board.
6. Slide the cover back to disengage the tab and lift the cover from the chassis.

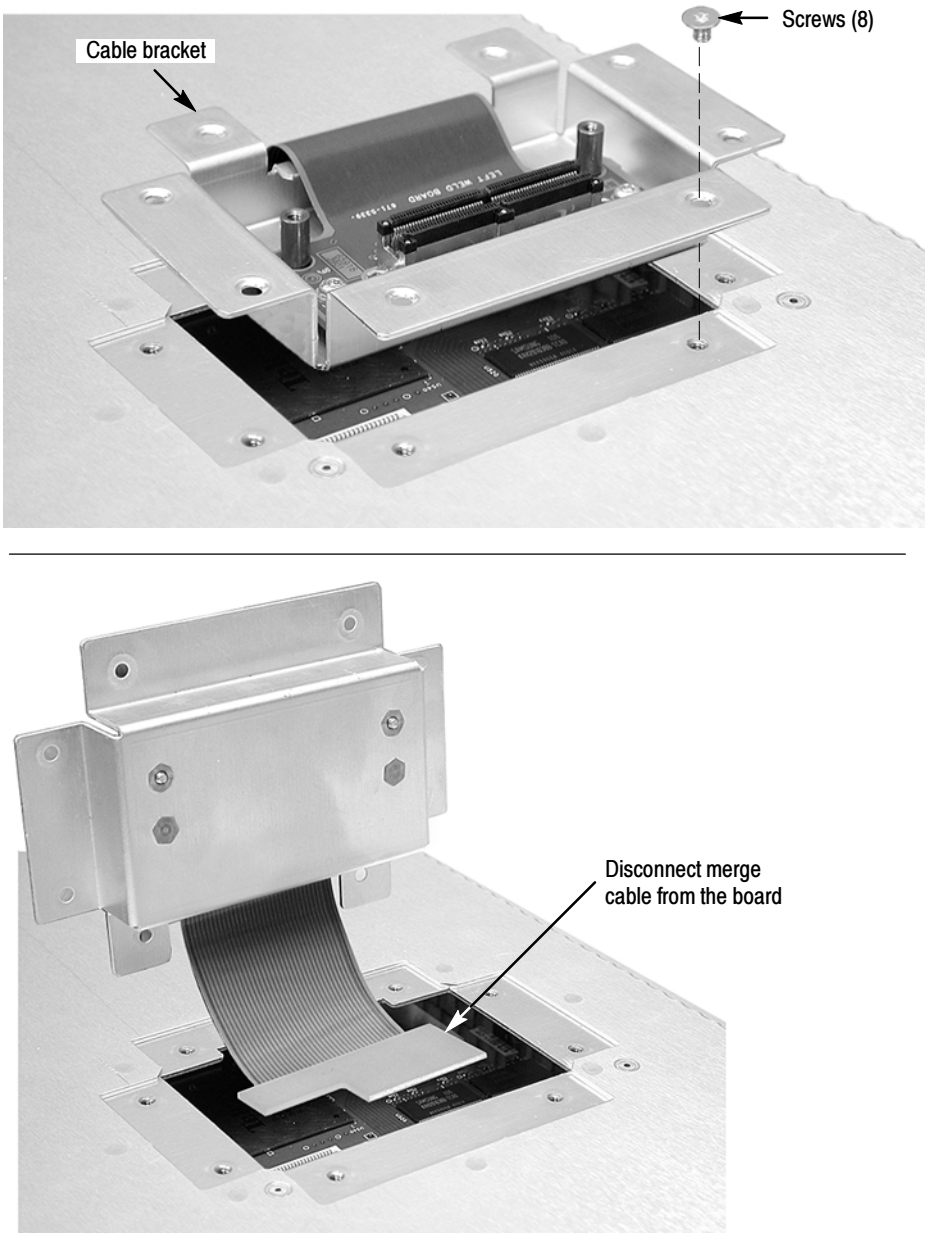


**Figure 6- 4: Removing the merge cable bracket from the cover**

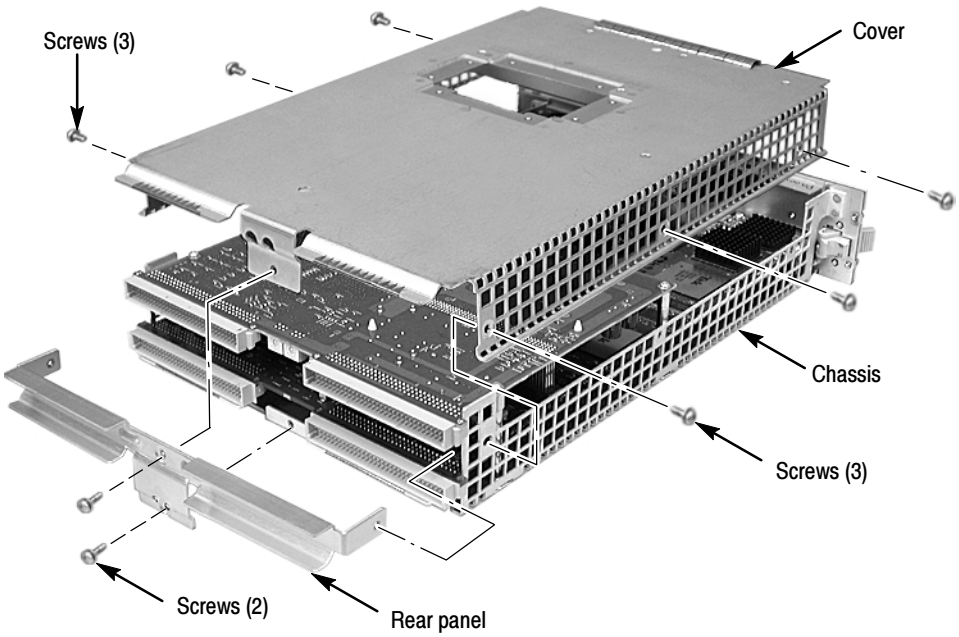


**Figure 6-5: Cover removal**

## Installation

Use the following procedure and Figures 6–4 through Figure 6–7 to install the covers:

***NOTE**. Install the cover tightly against the chassis. This will ensure that the module fits into adjacent slots in the mainframe.*

1. Place the module on its right side.

***CAUTION.** To prevent damage to the module during the installation process, reinstall the cover exactly as described in steps 2 through 8.*

*If the cover is not properly seated, the module can be damaged when you install it in a mainframe.*

2. Insert the cover at an angle (step 1 in Figure 6–6) such that the front edge of the cover engages with the EMI gaskets on the back of the front panel. Then push the rear of the cover in place (step 2 Figure 6–6).

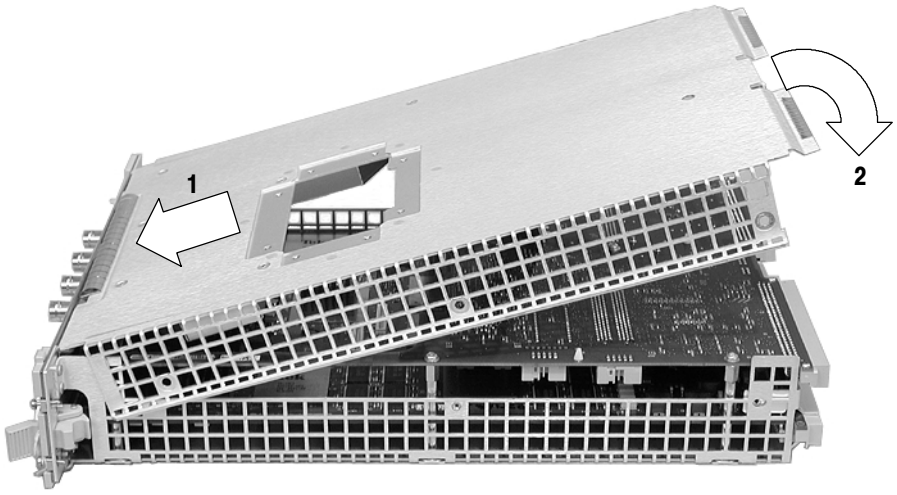


**Figure 6- 6: Installing the cover onto the chassis**

3. Make sure that the cover is fully seated (no gaps) against the front and rear chassis flanges (see Figure 6–7).
4. While holding the cover in place, install the four T-10 Torx-drive screws nearest the front of the module (two on each side of the cover), to secure the cover to the chassis.
5. Slide the rear panel on the chassis and install the two rear panel T-10 Torx-drive screws.
6. Gently squeeze the chassis flange and rear panels flange together while tightening the screws on the sides. This ensures that the rear panel does not rotate, otherwise the module may not seat properly when installed in the mainframe.
7. Install the two remaining T-10 Torx-drive screws nearest the rear of the module (one on each side of the cover).
8. Place the cover onto the chassis.
9. If your instrument has a merge cable, complete the following steps to install the merge cable assembly:
   a. Feed the merge cable through the cover.
   b. Carefully connect the merge cable to the circuit board (refer to Figure 6–4 on page 6–12 as necessary).
   c. Insert the bracket assembly into the hole in the cover.
   d. Install the eight T-9 countersunk screws on the bracket.

**10.** Check and tighten all screws to 4 in lbs.

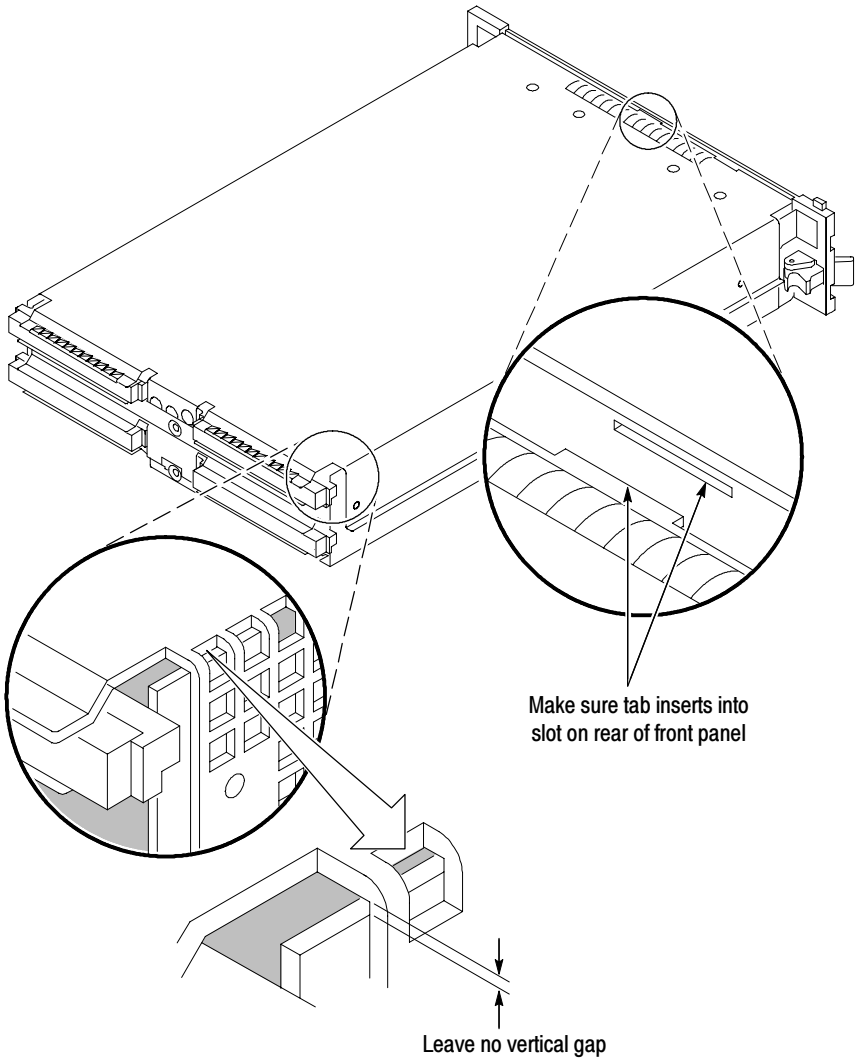


**Figure 6-7: Seating the cover on the chassis**

# Local Processor Unit Board

You will need a screwdriver with a T-10 tip to complete the following procedures.

***NOTE**. When placing an order for a replacement LPU board or an LPU exchange board from the Tektronix Exchange Center, you must supply the model number, serial number, PowerFlex Option upgrade number and firmware level.*

## Removal

Use the following procedure and Figure 6–8 to remove the LPU board:

1. Perform the *Cover* removal procedure (see page 6–11).
2. Remove the five T-10 Torx-drive screws that secure the LPU board to the chassis.

***CAUTION.** Handle the LPU board gently to avoid breaking the front panel LED extension.*

3. Carefully lift the LPU board up from the chassis to disengage the 160-pin connecter from the acquisition board.
4. Move the LPU board away from the front panel until the tabs (Figure 6–8) clear the front subpanel and then remove the LPU board from the chassis.

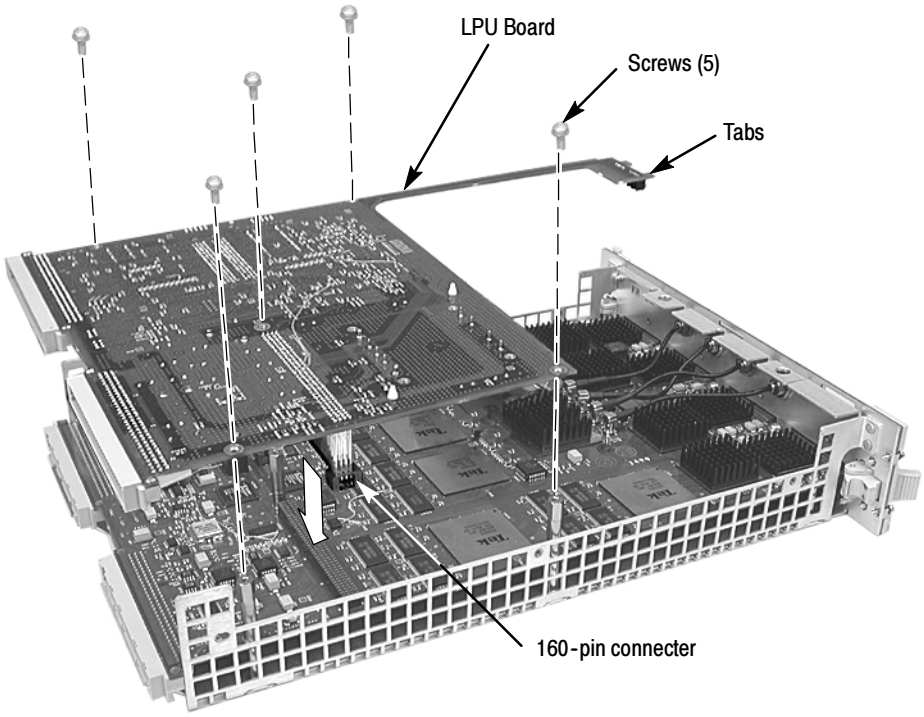


**Figure 6-8: LPU board removal**

## Installation

Use the following procedure and Figure 6–8 and Figure 6–9 to install the LPU board:

1. Place the LPU board (component side down) over the chassis and insert the tabs on the LPU board into the front subpanel as shown in Figure 6–9.
2. Line up the pins on the 160-pin connector from the LPU board to the acquisition board and gently press the LPU board in place.
3. Install the five T-10 Torx-drive screws that secure the LPU board to the chassis.
4. Perform the *Cover* installation procedure (see page 6–13).

***NOTE**. After replacing the LPU board, you must verify the proper PowerFlex level. The PowerFlex configuration information is listed on the side panel of the logic analyzer module. This information should match the module specific information on the System Properties tab in the TLA application.*

*If the PowerFlex level does not match the information on the side panel label, you must return the entire logic analyzer module to your local Tektronix service center.*

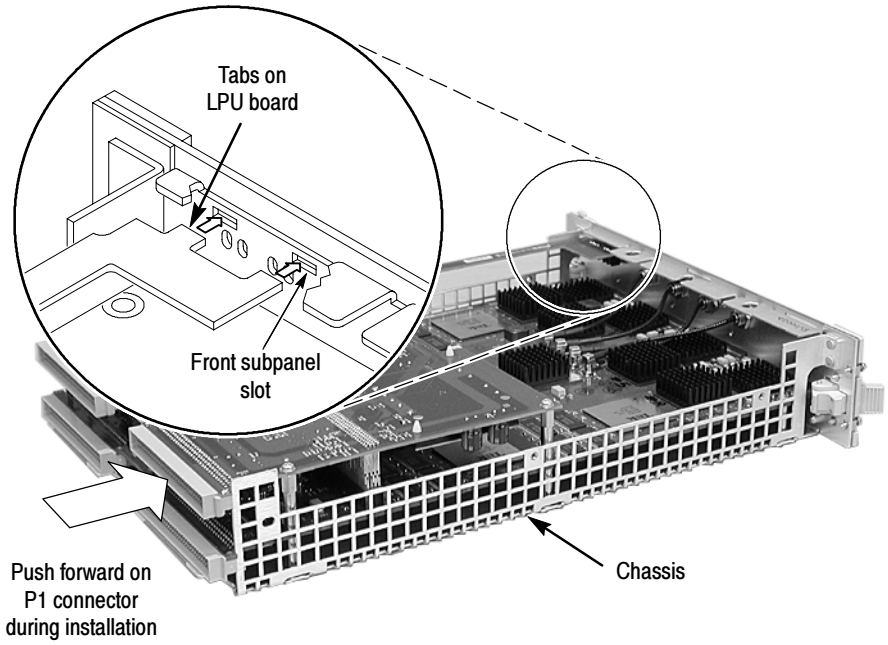


**Figure 6- 9: Inserting LPU board tabs into front subpanel**

# Acquisition Board

You will need a $^1/_4$ inch nut driver in addition to the T-10 Torx tip screwdriver to complete the following procedures.

## Removal

Use the following procedure and Figure 6–12 to remove the acquisition board:

1. Perform the *Cover* removal procedure (see page 6–11).
2. Perform the *Local Processor Unit Board* removal procedure (see page 6–16).

***NOTE**. The 34-channel and 68-channel modules do not have a left side or right side merge cable. For these modules, ignore the steps dealing with the merge cable.*

3. Complete the following steps while referring to Figure 6–10 and Figure 6–11 on page 6–20 to remove the merge cable assembly:
   a. Turn the chassis over and remove the two T-10 screws from the merge cable assembly bracket as shown in Figure 6–10.

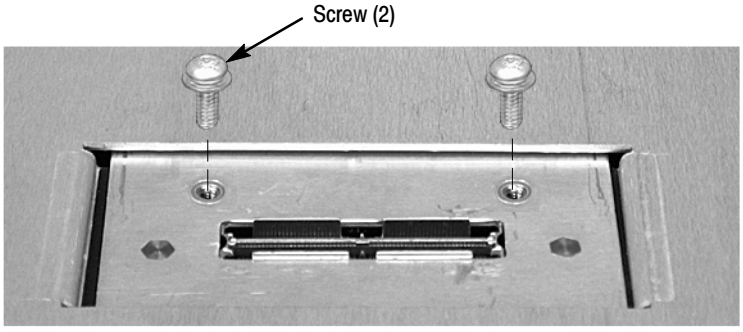


**Figure 6-10: Remove the single screw from the merge cable bracket**

   b. Carefully slide the bracket back underneath the cover until you can grasp the edge as shown in Figure 6–11.
   c. Lift the merge cable assembly bracket out of the hole being careful not to damage the assembly.
   d. Disconnect the merge cable from the acquisition board and set the assembly aside.

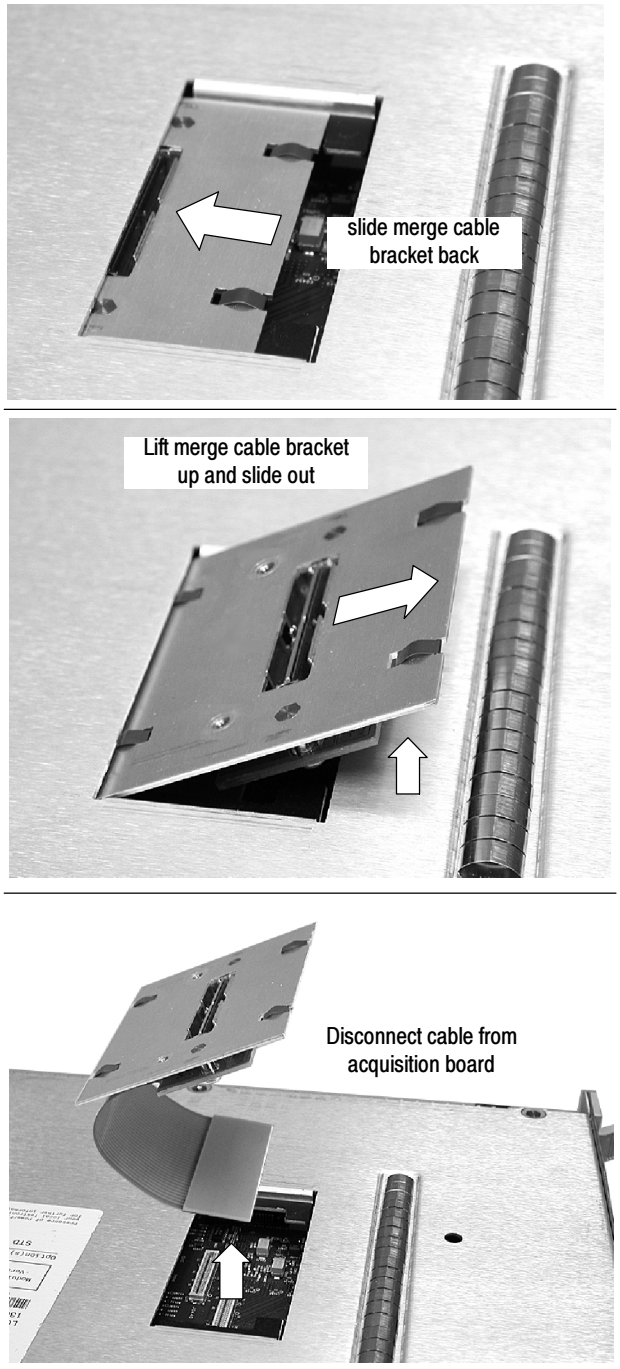


**Figure 6- 11: Removing the merge cable assembly**

4. Turn the chassis over and then remove the five spacer posts with the $^1/_4$ nut driver from the acquisition board.
5. Disconnect the four analog output cables on the acquisition board.
6. Remove the five T-10 screws from the acquisition board located near the front of the chassis.

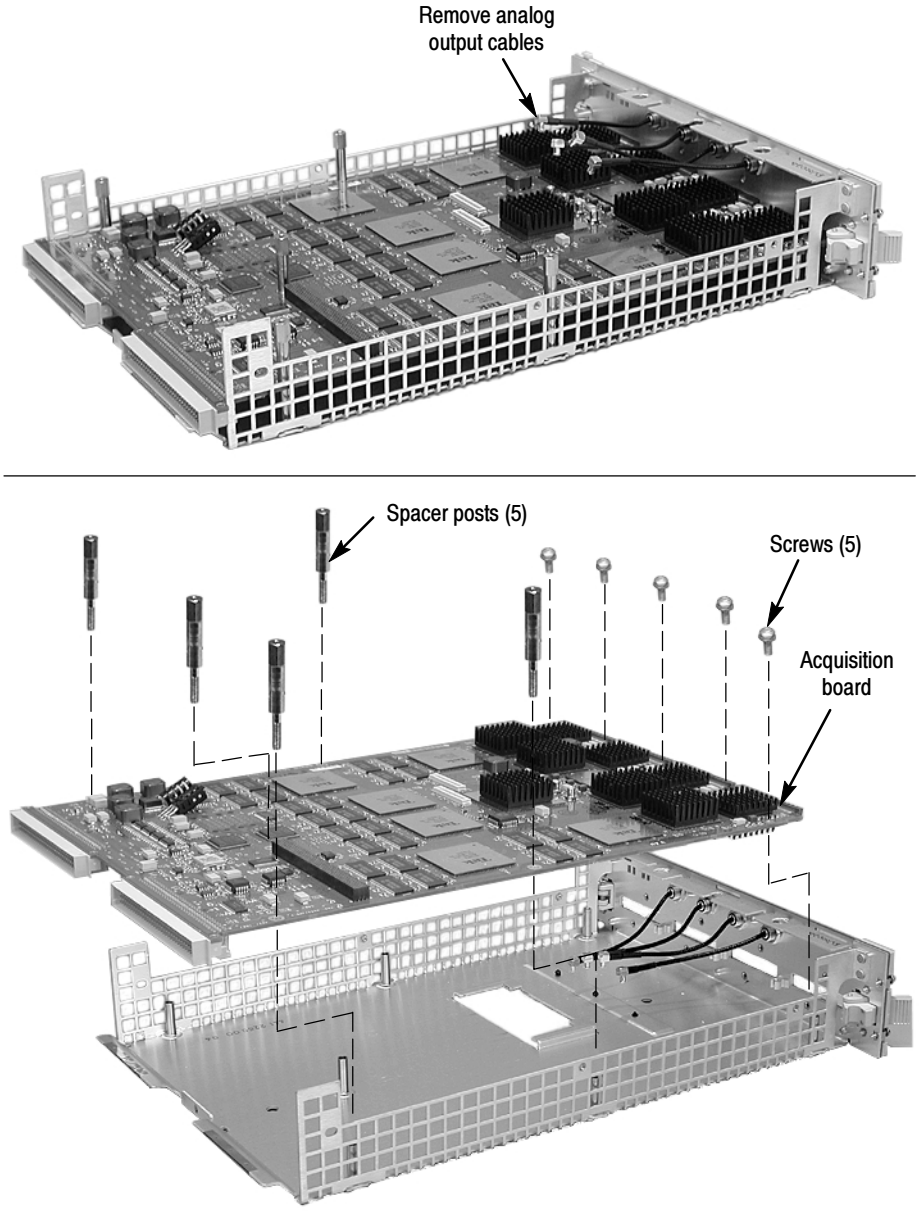


**Figure 6-12: Removing the acquisition board from the chassis**

7. Carefully slide the acquisition board away from the front panel until the probe connectors clear the front panel. Then lift the circuit board out of the chassis.

## Installation

Use the following procedure to install the acquisition board:

1. Place the acquisition board into the chassis.
2. Carefully slide the acquisition board into the chassis until the probe connectors fit snuggly into the front panel slots.
3. Install five T-10 screws on the acquisition board at the front of the chassis.
4. Install the five spacer posts that secure the acquisition board to the chassis.
5. Connect the four analog output cables from the front panel to the acquisition board.
6. Complete the following steps to install the merge cable assembly (skip these steps if your instrument does not have a merge cable assembly):
   a. Turn the chassis over.
   b. Feed the merge cable into the hole and connect it to the circuit board (refer to Figure 6–11 on page 6–20 if necessary).
   c. Carefully slide the merge cable assembly into the hole.
   d. Slide the bracket forward and install the tow T-10 screws to hold the bracket in place.
7. Perform the *Local Processor Unit Board* installation procedure (see page 6–17).
8. Perform the *Cover* installation procedure (see page 6–13).

## Fuses

There are no user-replaceable parts on any of the circuit boards. If you suspect that an open fuse exists, there is no easy way of determining the cause of the open fuse. Most of the fuses are surface mounted and attempting to change the fuses with improper tools will result in damaging the circuit boards beyond repair. You should return the circuit board to you local Tektronix service center for corrective action.

## Front and Rear EMI Gaskets

### Removal

Use the following procedure to remove the front and rear EMI gaskets:

1. Perform the *Cover* removal procedure (see page 6–11).
2. For the front EMI gaskets:
   a. Locate the gasket to be replaced.
   b. Lift the gasket fingers and rotate the gasket off.
3. For the two rear gaskets on the chassis
   a. Perform the *Local Processor Unit Board* removal procedure (page 6–16), and the *Acquisition Board* removal procedure (page 6–19).
   b. Lift the gasket fingers and rotate the gasket off (see Figure 6–13).

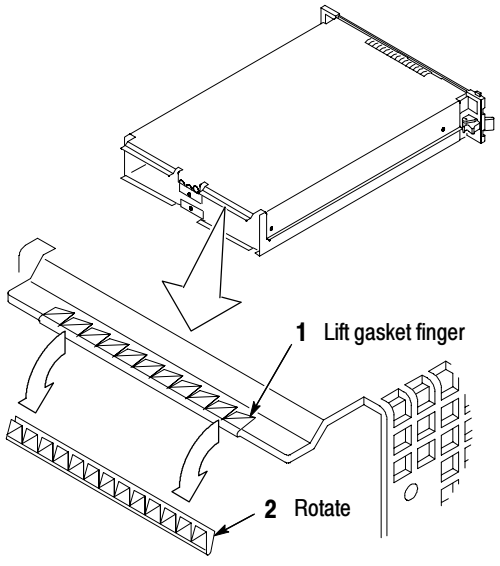


**Figure 6–13: Rear EMI gasket removal**

### Installation

Use the following procedure and Figure 6-14 to install the EMI gaskets:

1. Position each gasket so the gasket fingers face the outside of the module.

***CAUTION.*** *To avoid breaking the gasket fingers, do not lift the fingers too high.*

2. Pick up each gasket at the end where the gasket finger is formed up. Then rotate the gasket on. As you do this, lift up any fingers that bind to the chassis or cover.
3. Slide each gasket gently from side to side to ensure that the gasket snaps in place.

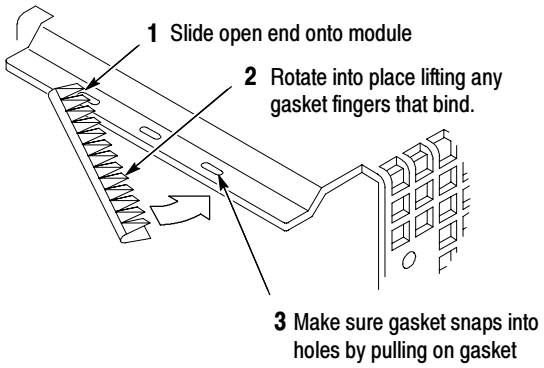


**Figure 6-14: Rear EMI gasket replacement**

4. Reinstall the Acquisition board and the LPU board if you removed them to install the rear EMI gaskets (see pages 6-17 and 6-22).
5. Install the module covers. (see page 6-13).

## Side EMI Gaskets

To remove the side EMI gaskets, remove the covers and circuit boards as necessary to access the EMI gaskets (refer to Figure 10-1 on page 10-4 for the gasket locations). Pop the EMI gaskets out of the cover.

To install the side EMI gaskets, pop them into place on the covers.

# Troubleshooting

***WARNING.*** *Before performing this or any other procedure in this manual, read the* General Safety Summary *and* Service Safety Summary *found at the beginning of this manual. Also, to prevent possible injury or damage to electrical components, read* Preventing Electrostatic Discharge *on page 6–1.*

This section contains information and procedures designed to help isolate faults to within the logic analyzer module. The process is as follows:

1. Review *Check for Common Problems*, beginning on page 6–26, to eliminate easy to find problems.
2. Perform procedures outlined in *Eliminate Other Problem Sources*, beginning on page 6–28, to eliminate the mainframe, probes, and other modules as the source of the fault(s).
3. Perform the *Troubleshoot the Logic Analyzer Module* procedure, beginning on page 6–29, to identify the failed replaceable part within the module.

If you replace a faulty circuit board or assembly found using these procedures, you must follow any verification and adjustment procedures identified in Table 6–6 on page 6–35 for the replaced board.

## Service Level

This section supports isolation of faults within the logic analyzer module to the replaceable-part level that's reflected in the replaceable parts lists in Chapter 10. In most cases, faults are isolated to circuit boards or assemblies, but not to individual components on those boards. (See *Strategy for Servicing* on page xix.)

Fault isolation is supported to the following circuit boards and replaceable parts:

- LPU board
- Acquisition board

## Required Documentation

You may need to refer to additional service manuals to isolate faults. In addition, other manuals and other sections in this manual contain instructions you will need to complete repairs after locating a faulty part. For a list of supplemental documentation, refer to the following table.

| Manual or Section | Purpose |
|---|---|
| *TLA715 Portable Mainframe Service Manual* or *TLA721 Benchtop Mainframe & TLA7XM Expansion Mainframe Service Manual* | To eliminate benchtop or portable mainframe as problem source (whichever configuration is in use) |
| *Tektronix Logic Analyzer Family User Manual* | To remove and reinstall modules in mainframe |
| *TLA7UP Mainframe Field Upgrade Instruction Manual* | To reinstall Windows 2000, the TLA application software on mainframes or to upgrade module firmware when required |

## Check for Common Problems

Use Table 6–4 to quickly isolate possible failures. The table lists problems related to the logic analyzer module and possible causes. The list is not exhaustive, but it may help you eliminate a problems that are easy to fix.

***CAUTION.*** *To avoid damaging the logic analyzer module or the mainframe, be sure to power down the mainframe before removing or reinstalling any modules.*

**Table 6-4: Failure symptoms and possible causes**

| Symptom | Possible cause(s) |
|---|---|
| Mainframe does not power on | ■ Power connection faulty; check or substitute power cord<br>■ Fuse blown; check line fuse<br>■ Mainframe power supply failure; contact local Tektronix service center<br>■ Mainframe controller is not installed properly (or not at all) |
| Mainframe does not boot | ■ Non-system disk or floppy in external drive; make sure logic analyzer boots from hard drive (Refer to the *Tektronix Logic Analyzer Family User Manual* for software reinstallation procedures)<br>■ Hard drive failure or corrupted files on hard drive; contact local Tektronix service center |
| Modules not recognized | ■ Modules not fully inserted; make sure front of module is flush with front panel<br>■ Mainframe power supply failure; contact local Tektronix service center<br>■ Corrupted module firmware; reinstall firmware. Refer to the *TLA7UP Mainframe Field Upgrade Instruction Manual* for information on reinstalling the latest firmware<br>■ Module logical address switches set to 00. Reset the switches to FF. |
| Controller does not power on | ■ Module not fully inserted; make sure front of module is flush with front panel<br>■ Module failure; try substituting a known-good controller module and if necessary, contact local Tektronix service center |
| Module does not pass the normal power on diagnostics (READY indicator not green) | ■ Module not fully inserted; make sure front of module is flush with front panel<br>■ Module failure; see *Troubleshoot the Logic Analyzer Module*, or contact local Tektronix service center<br>■ Open fuses on logic analyzer module circuit boards |
| Module loses settings when power is turned off | ■ Module failure; see *Troubleshoot the Logic Analyzer Module*, or contact local Tektronix service center<br>■ NV RAM failure; refer to page 6-16 for local processor unit board replacement instructions |
| Module will not acquire data or the acquired data is incorrect | ■ Module failure; see *Troubleshoot the Logic Analyzer Module*, or contact local Tektronix service center<br>■ Faulty probe, leadset, or probe adaptor |

## Eliminate Other Problem Sources

The logic analyzer module is part of the Tektronix Logic Analyzer Family, which consists of modules installed in either a benchtop or portable mainframe. The following procedures will help you eliminate the mainframe and other modules as possible sources of failures.

### Substitute a Good Module

If you have available a known-good logic analyzer module, perform the following procedure:

1. Remove the suspect logic analyzer module from the mainframe.
2. Install a known-good logic analyzer module in the same slot as the suspected module (verify that address switches on the rear of the module are set to same address as the module that you are replacing).
3. Power-on the logic analyzer and check for normal operation.
4. If the failure symptoms are still present with the known-good logic analyzer module installed, the problem most likely is in the mainframe or in the attached probes, not in the logic analyzer module.
5. To eliminate the probes, use known-good probes and verify that the probes are properly connected to the target system.

---

***NOTE.*** *Viewing the diagnostic window from the TLA application may help you isolate failures to individual modules or to the mainframe.*

---

6. If the logic analyzer operates normally with the known-good logic analyzer module and with known-good probes, the suspect logic analyzer module needs to be repaired. Refer to *Troubleshooting the Logic Analyzer Module* on page 6–29 for additional troubleshooting procedures.

### Probe-Level Troubleshooting

If the logic analyzer module acquires no data or faulty data, the probes may be at fault. Perform the following procedure to isolate faults to a probe or to the logic analyzer module.

---

***NOTE.*** *The procedure below requires that the logic analyzer is functional and operates normally when the modules are installed.*

---

1. Verify that the probe is correctly connected to the module and to the target system.

2. Move the suspected probe to another probe connector and observe if the problem follows the probe. If the problem does not follow the probe, the module may be faulty.
3. Substitute the suspected probe with a known good probe and observe if the problem is still present. If the problem still occurs, the module may be faulty. Refer to *Troubleshoot the Logic Analyzer Module* to isolate the problems within that module.
4. If you are using a general purpose probe with lead sets and you have determined that the probe is faulty, try to isolate the problem to an individual channel. A faulty channel may indicate a faulty probe podlet. Isolate faulty podlets by switching single podlets and observing if the problem tracks with the suspected podlet.

## Troubleshoot the Logic Analyzer Module

Follow the procedure in this section to identify the failed part within the logic analyzer module.

This procedure requires that the module is installed in a fully functional mainframe. If you have not determined that the mainframe is functional, or if you suspect the problem might be in a probe or in another module, refer to *Eliminating Other Problem Sources*.

### Equipment Required

The basic troubleshooting procedures require minimal test equipment. There are no accessible test points to measure voltages. An ohmmeter is recommended for checking fuses.

### Preparation

The fault isolation procedure requires that you:

- Recognize codes flashed by the front-panel LEDs during power up
- Are familiar with the power-on diagnostics

To fill these requirements, read the topics below before performing the *Fault Isolation Procedure* on page 6–31.

### Calibration and Diagnostic Procedures

The following calibration and diagnostic procedures will help you diagnose problems.

**Self Calibration.** Use self calibration to calibrate the installed modules. Run the self calibration after a minimum of a 30 minute warm-up and prior to running the extended diagnostics. For more information on when to run the self calibration, refer to *Self Calibration* on page 5–5.

**Power-On Diagnostics.** Power-on diagnostics check basic functionality of the logic analyzer at every power on. If any failures occur at power on, the screen displays the calibration and diagnostics property sheet.

If there are no diagnostic failures when you power on the logic analyzer, you can display and run the calibration and diagnostics property sheet by selecting Calibration and Diagnostics from the System menu.

**Extended Diagnostics.** The extended diagnostics execute more thorough tests than the power-on diagnostics. Using the extended diagnostics, you can do the following tasks:

- Run tests individually or as a group
- Run tests once or continuously
- Run tests until failures occur

---

***NOTE.*** *Certain diagnostic tests will fail if probes are attached. For best results, run the diagnostics with probes disconnected from the module.*

---

To run the extended diagnostics, do the following steps:

1. Disconnect the probes from the logic analyzer module.
2. Start the TLA application if it is not already running.
3. From the System menu, select Calibration and Diagnostics.
4. Select the Extended Diagnostics property page.
5. Select the individual tests, group of tests, or all tests.
6. Click the Run button.

While the tests are executing, the word Running displays adjacent to the tests. When the tests are complete, either a Pass or Fail indication displays adjacent to each test.

**Merged Modules.** The extended diagnostics include a special merge test that verifies the correct pipeline adjustment for the master module, inside slave module, and outside slave module. This test does not require the modules to be physically merged together.

Every time modules are merged in the System Configuration window, a calibration is performed between the merged modules. An error message will appear if there are any problems with the merge cables, circuit board traces, of if the calibration fails.

## Fault Isolation Procedure

The Primary Troubleshooting Tree (Figure 6–15 on page 6–32) provides troubleshooting steps that test the logic analyzer module. Use the following procedure with that tree:

To determine if module is recognized, perform the following steps:

1. Install the logic analyzer module into a known-good mainframe.
2. Before you power on the mainframe, look at the READY, ACCESSED ARM'D, and TRIG'D front panel indicators.
3. Power on the mainframe and note how the front panel indicators respond.
   a. Verify that the green READY indicator turns on while the diagnostics are being checked. If the green READY indicator does not turn on, the module is not being recognized which indicates possible problems on the LPU board.
   b. Verify that after a few seconds the ACCESSED indicator turns on. The indicator stays on while the module is accessed by the controller. After the System window displays, the indicator blinks anytime the controller accesses the module.
4. If steps 3a and 3b are verified, the module is recognized; if not verified, the module is not recognized. Proceed as the troubleshooting tree instructs.
5. If diagnostic failures occur, replace the circuit board indicated by the troubleshooting tree. For further confirmation, you can correlate the failed test displayed with a board using Table 6–5 on page 6–33. *You should also first check the "special cases" of diagnostic failures below:*
   - Note from the tree, that if all the diagnostics pass, but self calibration fails, replace the Acquisition board.
   - If any of the Kernel test groups fail (ROM check, LPU RAM, LPU Address decode, etc.) replace the LPU board.
   - If the kernel group passes, but there are other failures, replace the Acquisition board. Also, ensure that the probes are disconnected from the module before running the diagnostics.
   - If multiple tests fail, the problem could be power-supply related problems or the mainframe. If replacing the Acquisition board does not remedy the failures, try replacing the LPU board.

***NOTE**. Due to the module design, there are no accessible test points on the module to connect external test equipment, to help isolate faults to an individual circuit board.*

6. Use the *Removal and Installation Procedures* that begin on page 6–9 to replace the faulty circuit board.
7. Refer to Table 6–6 on page 6–35 after module replacement and perform *all* verification and adjustment procedures identified for the replaced module.

## Primary Troubleshooting Chart

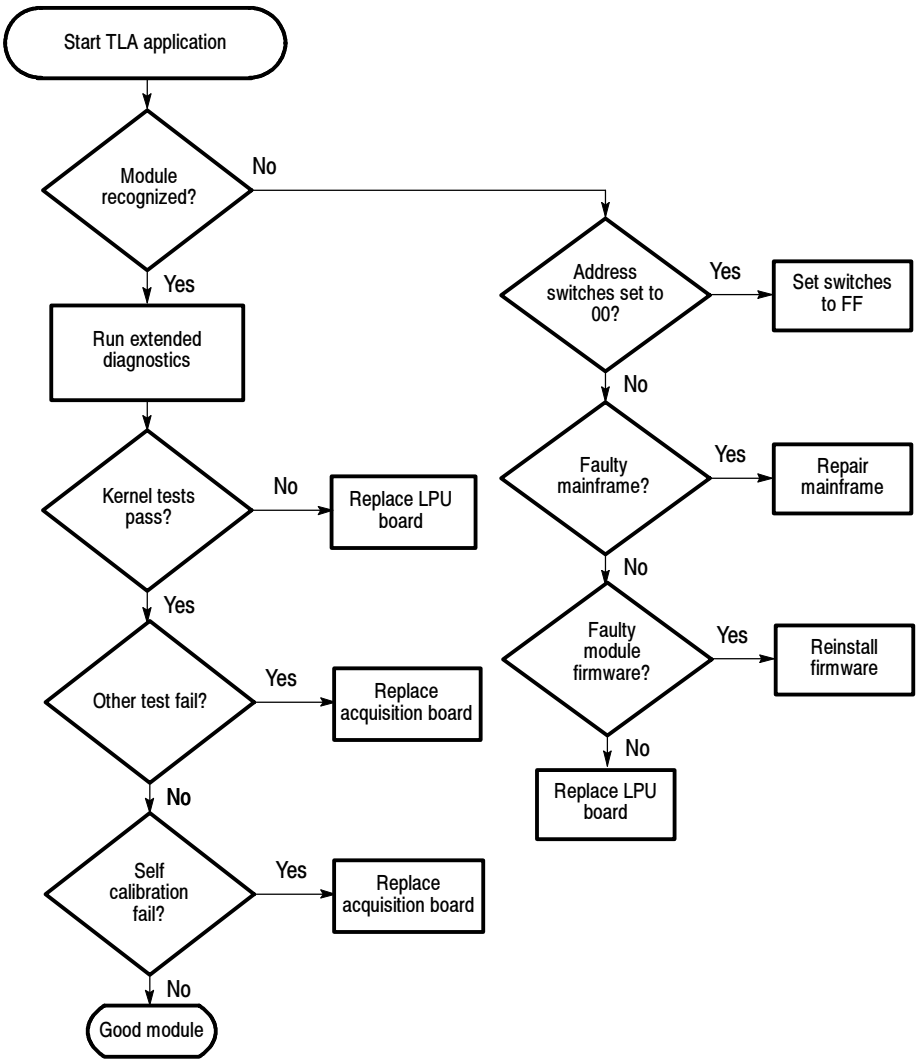


**Figure 6-15: Primary troubleshooting chart**

## Diagnostics Table

Table 6–5 can help you isolate problems to one of the circuit boards in the module (use the *Removal and Installation Procedures* beginning on page 6–9 to replace the faulty circuit board):

**Table 6-5: Diagnostic tests**

| Circuit board | Group & test | Power on | Extended |
|---|---|---|---|
| LPU board | Kernel | | |
| | ROM Check | ✓ | ✓ |
| | LPU RAM | ✓ | ✓ |
| | Address Decode | ✓ | ✓ |
| | NVRAM Check | ✓ | ✓ |
| Acquisition board | Timestamp | | |
| | Timestamp Rollover | ✓ | ✓ |
| | Acquisition RAM Data Bus | ✓ | ✓ |
| | Acquisition RAM Address Bus | ✓ | ✓ |
| | Timestamp Acquire | | ✓ |
| | Clock | | |
| | Qualifier/Combiner RAM | ✓ | ✓ |
| | Clock State Machine RAM | ✓ | ✓ |
| | Acquisition Data Path | | |
| | Address/Data Bus | ✓ | ✓ |
| | MagniVu RAM | | ✓ |
| | Trigger | | |
| | Internal RAM | ✓ | ✓ |
| | Trigger Crossbar | ✓ | ✓ |
| | Signal/Trigger Lines | ✓ | ✓ |
| | Trigger State Machine Counters | ✓ | ✓ |
| | Prefill Counter | ✓ | ✓ |
| | Word Recognizer | ✓ | ✓ |
| | Transition Detector | ✓ | ✓ |
| | Clock Group Detector | ✓ | ✓ |
| | At-speed Transition Detect | | ✓ |
| | Snapshot | | ✓ |
| | Acquisition RAM | | |
| | RAM Select | ✓ | ✓ |
| | Acquisition Memory | | ✓ |

**Table 6-5: Diagnostic tests (Cont.)**

| Circuit board | Group & test | Power on | Extended |
|---|---|---|---|
| Acquisition board | Miscellaneous Tests | | |
| | Acquisition Address Decode | ✓ | ✓ |
| | Threshold | ✓ | ✓ |
| | At-speed Async Acquire | | ✓ |
| | Pseudo Random | | ✓ |
| | SFDL-1 | ✓ | ✓ |
| | SFDL-2 | ✓ | ✓ |
| | PLL | ✓ | ✓ |
| | Demux | | ✓ |
| | Edge Detector | | ✓ |
| | Setup and Hold | | ✓ |
| | Glitch | | ✓ |
| | Memory Interface Controller | | |
| | AD Bus | ✓ | ✓ |
| | MAR Rollover | ✓ | ✓ |
| | Waveform 0 | ✓ | ✓ |
| | Waveform 1 | ✓ | ✓ |
| | Waveform Pins | ✓ | ✓ |
| | Waveform Change | ✓ | ✓ |
| | Search Stack | ✓ | ✓ |
| | Internal Search | ✓ | ✓ |
| | External Search | ✓ | ✓ |
| | Counters | ✓ | ✓ |
| | RAM Data | ✓ | ✓ |
| | RAM Address | ✓ | ✓ |
| | High-Speed Memory Compare | ✓ | ✓ |
| | Pattern Acquire | | ✓ |
| | Miscellaneous 2 Tests | | |
| | Counters | | ✓ |
| | Timers | | ✓ |
| | Store Stretch | | ✓ |
| | Range Recognizer | | ✓ |
| | Global Storage | | ✓ |
| | CSM Input Path | | ✓ |

## Adjustment After Repair

After the replacing a circuit board or assembly due to electrical failure, locate the board removed in Table 6–6 and perform the indicated procedures.

**Table 6-6: Requirements after replacement**

| Board replaced | Adjustment required | Verification checks |
|---|---|---|
| LPU board | Adjustment: Powerflex[1], Firmware level restoration[2], Deskew, Self Calibration, Threshold tests | Self Calibration, Power-on and Extended Diagnostics, performance verification procedures |
| Acquisition board | Adjustment: Self Calibration, Deskew, Threshold tests | Self Calibration, Power-on and Extended Diagnostics, performance verification procedures |

[1] **The PowerFlex restoration or changes can only be made by Tektronix service personnel.**

[2] **Refer to the *TLA7UP Mainframe Field Upgrade Instruction Manual* for instructions for updating module firmware.**

## Updating or Restoring the Logic Analyzer Firmware

You may have to update the firmware on the logic analyzer module if the module does not appear in the TLA System window after you have serviced the module or after you have updated the TLA application software on the mainframe. You can update multiple modules and module types during a single firmware update session. The most current firmware resides on a file on the hard disk of the logic analyzer mainframe.

1. Note which of the modules that may require new firmware.

   If any modules are missing from the System window, you can verify the status of the modules by doing the following steps:

   a. Select System Properties from the System menu.

   b. Click the Modules tab.

   c. Note the information under the Messages column for any installed modules. If any modules indicate invalid or similar messages, you must update the firmware for those modules.

2. Disconnect any probes connected to the modules that you want to update.

3. Exit the logic analyzer application.

4. Click Start → Programs → Tektronix Logic Analyzer → TLA Firmware Loader.
5. When you see the pop-up prompting you to cycle the power on the mainframe after completing the upgrade operation, click Yes.

   The logic analyzer will scan the mainframe to determine which modules are installed and which modules can have their firmware upgraded. If you have any older modules, you may see them listed in the bottom half of the window. These modules cannot be updated until you install the flash jumper on the rear of the modules.
6. Select the modules that you want to update from the list of modules displayed in the Supported list box near the top of the window. If you are updating more than one module at a time, note the slot location of the module in the selection box.
7. Select Load Firmware from the Execute menu.
8. Click the TLA7A.lod file for the selected module.

***NOTE.*** *Be sure to select the proper .lod file for each module. Note the slot number in the title bar so that you select the correct module for the .lod file.*

9. Click OK. You will be asked to confirm your action; click Yes when prompted.

***NOTE.*** *The program will not allow you to load firmware to an incompatible module. For example, the program will not load DSO firmware to a logic analyzer module.*

   The program will load the firmware for each module one at a time. The process may take several minutes per module.
10. Exit the firmware loader program and power down the logic analyzer. You must power down the logic analyzer to allow the TLA application to start up properly.
11. Remove the logic analyzer module from the mainframe.
12. Locate the big label on the side of the module.
13. Record the firmware version that is printed on the label. You will need this information to see that the firmware version matches the label.
14. Reinstall the module in the mainframe and power on the mainframe.

15. After the logic analyzer completes the power-on diagnostics, select System Properties from the System menu.
16. Click the module tab (for example, LA1).
17. Verify that the firmware version for the selected module matches the version on the label that you recorded in step 13.
18. If the firmware versions do not match, power down the mainframe, remove the module from the mainframe and update the label.

## Overview of Procedures

Table 6–7 provides a brief overview of the troubleshooting, adjustment, verification, and calibration procedures.

***NOTE**. Calibration constants are stored in the LPU NVRAM. You must always perform a new self calibration, complete the adjustment procedures, complete the performance verification procedures, and complete the certification procedures after you replace the LPU board.*

**Table 6-7: Troubleshooting overview**

| Procedure | Recommended interval | Purpose | When required | Documented |
|---|---|---|---|---|
| Diagnostics (power on and extended) | Incoming inspection<br>Annually | Verifies basic functionality. | During troubleshooting | *Power on Diagnostics*, page 6–30 |
| Adjustment: self calibration and performance verification | Annually<br>As needed | Verifies basic functionality. | After board replacement | *Self Calibration*, page 5–5 and *Performance Verification procedures* |
| Adjustment: deskew | After board replacement or annually | Time-aligns the data channels | After board replacement | *Performance Verification* and *Adjustment Procedures* |
| Functional verification | Incoming inspection<br>As needed | Verifies front end and basic functionality including probes | After board replacement | *Performance Verification* and *Adjustment Procedures* |
| Performance verification | Annually or as needed | Verifies advertised performance specifications | After board replacement | *Performance Verification* and *Adjustment Procedures* |
| Calibration (certification) | Annual recertification | Verifies primary references | After board replacement | *Performance Verification* and *Adjustment Procedures* |

# Repackaging Instructions

This section contains the information needed to repackage the logic analyzer module for shipment or storage.

## Packaging

If at all possible use the original packaging to ship or store the instrument. If the original packaging is not available, use a corrugated cardboard shipping carton having a test strength of at least 275 pounds (125 kg) and with an inside dimension at least six inches (15.25 cm) greater than the instrument dimensions. Add cushioning material to prevent the instrument from moving around in the shipping container. Seal the shipping carton with an industrial stapler or strapping tape.

## Shipping to the Service Center

Contact the Service Center to get an RMA (return material authorization) number, and any return or shipping information you may need.

If the instrument is being shipped to a Tektronix Service Center, enclose the following information:

- The RMA number.
- The owner's address.
- Name and phone number of a contact person.
- Type of instrument and serial number.
- Reason for returning.
- A complete description of the service required.

***NOTE**. When ordering the LPU board for exchange or repair, you will need to supply the above information, including the firmware level and PowerFlex configuration information.*

Mark the address of the Tektronix Service Center and the return address on the shipping carton in two prominent locations.

***CAUTION.*** *When returning the LPU board separately, be sure to properly support the narrow LED arm of the circuit board so it will not be damaged during transit or storage.*

## Storage

The logic analyzer module should be stored in a clean, dry environment. The following environmental characteristics apply for both shipping and storage:

- Temperature range: –40 °F to +160 °F (–40 °C to +71 °C).
- Altitude: To 40,000 feet (12,190 meters).

See Table 1–9 on page 1–12 for a complete listing of the module environmental characteristics.

# Options

This chapter lists the advertised options for each logic analyzer module. Refer to the *Mechanical Parts List* chapter for a list of standard and optional accessories for each module.

## TLA7AA1, TLA7AA2, TLA7AA3 and TLA7AA4 Options

Table 7–1 lists the options for the TLA7AA1, TLA7AA2, TLA7AA3 and TLA7AA4 modules. The number of probes per option depend on the number of channels in the logic analyzer module.

**Table 7-1: TLA7AA1, TLA7AA2, TLA7AA3 and TLA7AA4 options**

| Option | Description |
|---|---|
| 2P | Add P6810 Probes |
| 3P | Add P6860 Probes |
| 4P | Add P6880 Probes |
| 1S | Increase to 512 Kb memory depth @ 120 MHz state speed |
| 2S | Increase to 2 Mb memory depth @ 120 MHz state speed |
| 3S | Increase to 8 Mb memory depth @ 120 MHz state speed |
| 4S | Increase to 32 Mb memory depth @ 120 MHz state speed |
| 5S | Increase to 128 Kb memory depth @ 235 MHz state speed |
| 6S | Increase to 512 Kb memory depth @ 235 MHz state speed |
| 7S | Increase to 2 Mb memory depth @ 235 MHz state speed |
| 8S | Increase to 8 Mb memory depth @ 235 MHz state speed |
| 9S | Increase to 32 Mb memory depth @ 235 MHz state speed |
| AS | Increase to 128 Kb memory depth @ 450 MHz state speed |
| BS | Increase to 512 Kb memory depth @ 450 MHz state speed |
| CS | Increase to 2 Mb memory depth @ 450 MHz state speed |
| DS | Increase to 8 Mb memory depth @ 450 MHz state speed |
| ES | Increase to 32 Mb memory depth @ 450 MHz state speed |

## TLA7AB2 and TLA7AB4 Options

Table 7–2 lists the options for the TLA7AB2 and TLA7AB4 modules; the number of probes per option depend on the number of logic analyzer channels.

**Table 7-2: TLA7AB2 and TLA7AB4 options**

| Option | Description |
|---|---|
| 2P | Add P6810 Probes |
| 3P | Add P6860 Probes |
| 4P | Add P6880 Probes |
| 1S | Increase to 64 Mb memory depth @ 235 MHz state speed |
| 2S | Increase to 64 Mb memory depth @ 450 MHz state speed |

## Service Options

Tektronix Service Options are available at the time you order your instrument. Contact your local Tektronix Sales Office for more information.

| | | |
|---|---|---|
| Product installation service[1] | Option IN | Provides initial product installation/configuration and start-up training session including front panel and product familiarization. |
| Three years of calibration services | Option C3 | Provides factory calibration certification on delivery, plus two more years of calibration coverage. The instrument will be calibrated according to its calibration interval. |
| Five years of calibration services | Option C5 | Provides factory calibration certification on delivery, plus four more years of calibration coverage. The instrument will be calibrated according to its calibration interval. |
| Test data | Option D1 | Provides initial Test Data Report from factory on delivery. |
| Test data | Option D3 | Provides test data on delivery plus a Test Data Report for every calibration performed during 3 years of coverage – requires Option C3. |
| Test data | Option D5 | Provides test data on delivery plus a Test Data Report for every calibration performed during 5 years of coverage – requires Option C5. |
| Three years repair coverage | Option R3 | Extends product repair warranty to three years. |
| Five years repair coverage | Option R5 | Extends product repair warranty to five years. |

[1] **Availability of installation and on-site services depends on the type of product and may vary by geography.**

# Electrical Parts List

Refer to the *Mechanical Parts List* chapter for a complete list of replaceable parts.

# Diagrams

This chapter contains the block diagrams of the logic analzyer module. Use these diagrams in conjunction with the *Theory of Operation* to help you troubleshoot the module.

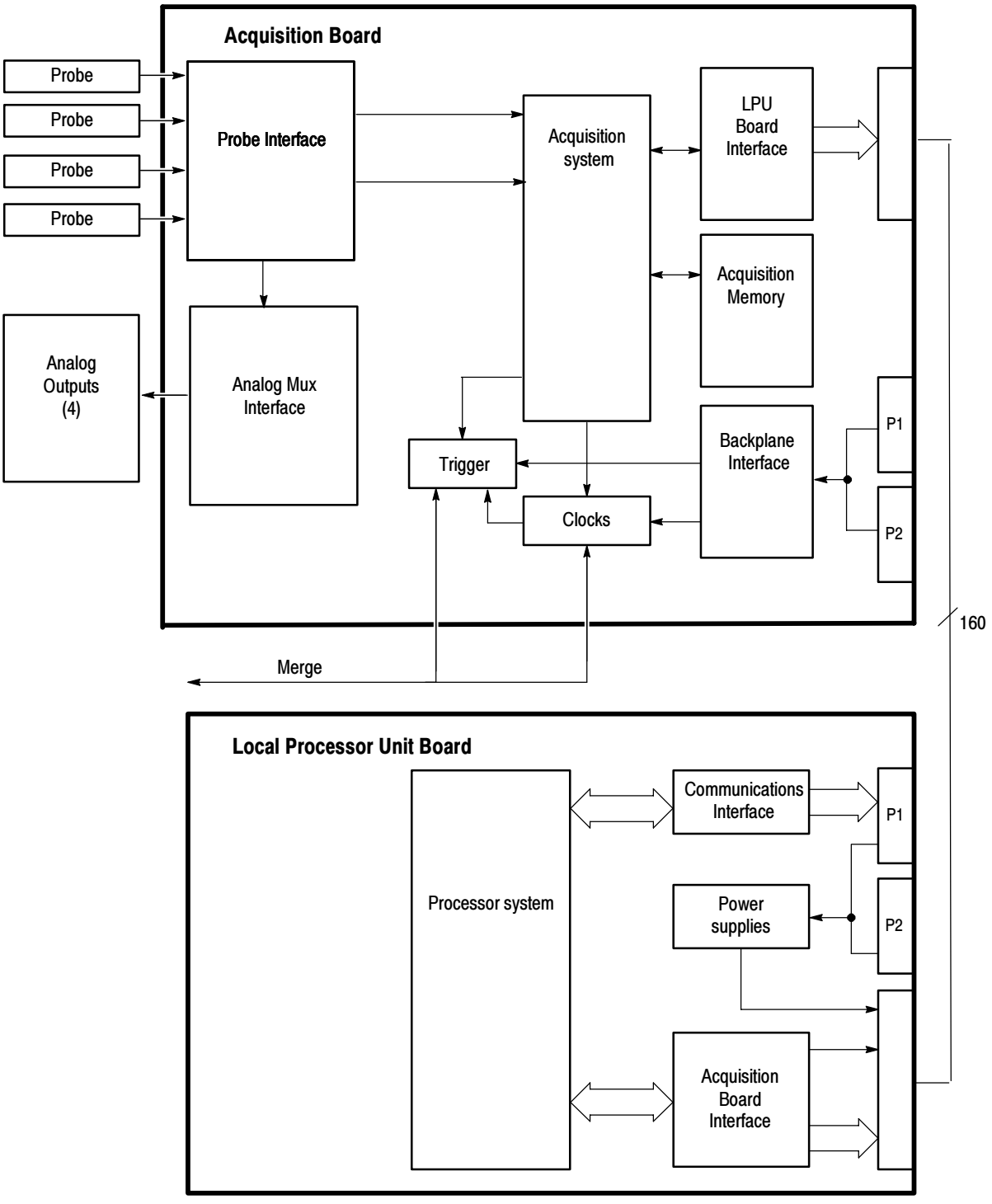


**Figure 9-1: Logic analyzer block diagram**

# Mechanical Parts List

This chapter contains a list of the replaceable parts for the Tektronix logic analyzer module. Use this list to identify and order replacement parts, modules, and subcomponents.

## Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

### Module Servicing

Modules can be serviced by selecting one of the following three options. Contact your local Tektronix service center or representative for repair assistance.

**Module Exchange.** In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-833-9200. Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices: www.tektronix.com.

**Module Repair and Return.** You may ship your module to us for repair, after which we will return it to you.

**New Modules.** You may purchase replacement modules in the same way as other replacement parts.

## Using the Replaceable Parts List

This section contains a list of the mechanical and/or electrical components that are replaceable for the logic analyzer module. Use this list to identify and order replacement parts. The following table describes each column in the parts list.

**Parts list column descriptions**

| Column | Column name | Description |
|---|---|---|
| 1 | Figure & index number | Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow. |
| 2 | Tektronix part number | Use this part number when ordering replacement parts from Tektronix. |
| 3 and 4 | Serial number | Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers. |
| 5 | Qty | This indicates the quantity of parts used. |
| 6 | Name & description | An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification. |
| 7 | Mfr. code | This indicates the code of the actual manufacturer of the part. |
| 8 | Mfr. part number | This indicates the actual manufacturer's or vendor's part number. |

### Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1-1972.

### Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

## Manufacturers cross index

| Mfr. code | Manufacturer | Address | City, state, zip code |
|---|---|---|---|
| 00779 | TYCO ELECTRONICS CORPORATION | CUSTOMER SERVICE DEPT<br>PO BOX 3608 | HARRISBURG, PA 17105-3608 |
| 060D9 | TENSOLITE COMPANY | PRECISION HARNESS AND ASSEMBLY<br>3000 COLUMBIA HOUSE BLVD<br>#120 | VANCOUVER, WA 98661 |
| 06915 | RICHCO | 5825 N TRIPP AVE<br>P.O. BOX 804238 | CHICAGO, IL 60646 |
| 09353 | C & K COMPONENTS CORP | 57 STANLEY AVE | WATERTOWN, MA 02172-4802 |
| 0KB01 | STAUFFER SUPPLY CO | 810 SE SHERMAN | PORTLAND, OR 97214-4657 |
| 0KB05 | NORTH STAR NAMEPLATE INC | LABEL PRODUCTS<br>5750 NE MOORE COURT | HILLSBORO, OR 97124-6474 |
| 0KM03 | LAIRD TECHNOLOGIES | 505 PORTER WAY | PLACENTIA, CA 92870 |
| 0MS63 | QT OPTOELECTRONICS | 610 N MARY AVENUE | SUNNYVALE, CA 94086 |
| 1AW87 | LEWIS SCREW CO. | 4300 SOUTH RACINE AVENUE | CHICAGO, IL 60609 |
| 24931 | FCI USA INC | RF/COAXIAL DIV<br>2100 EARLYWOOD DR<br>PO BOX 547 | FRANKLIN, IN 46131 |
| 51506 | ACCURATE SCREW MACHINE CORPORATION (ASM CO) | 10 AUDREY PLACE | FAIRFIELD, NJ 07004-6095 |
| 61058 | PANASONIC INDUSTRIAL CO ECG | M/S 7H-4<br>TWO PANASONIC WAY | SECAUCUS, NJ 07094 |
| 61935 | SCHURTER INC | 1016 CLEGG CT<br>PO BOX 750158 | PETALUMA, CA 94975-0158 |
| 71400 | BUSSMANN | DIVISION COOPER INDUSTRIES INC<br>PO BOX 14460 | ST LOUIS, MO 63178 |
| 7X318 | KASO PLASTICS INC | 5720-C NE 121ST AVE, STE 110 | VANCOUVER, WA 98682 |
| 80009 | TEKTRONIX INC | 14150 SW KARL BRAUN DR<br>PO BOX 500 | BEAVERTON, OR 97077-0001 |
| 81073 | GRAYHILL INC | 561 HILLGROVE AVE<br>PO BOX 10373 | LAGRANGE, IL 60525 |
| 83330 | DIALIGHT CORP | MANASQUAN DIV<br>1913 ATLANTIC AVE | MANASQUAN, NJ 08736-1005 |
| S3109 | FELLER U.S. CORPORATION | 68 VERONICA AVE, UNIT #5 | SOMERSET, NJ 08873 |
| TK0212 | MURATA MFG CO LTD | TJBO LIAISON<br>M/S 78-210 | BEAVERTON, OR 97077 |
| TK0588 | UNIVERSAL PRECISION PRODUCT | 1775 NW CORNELIUS PASS RD | HILLSBORO, OR 97124 |
| TK1943 | NEILSEN MANUFACTURING INC | 3501 PORTLAND RD NE | SALEM, OR 97303 |
| TK1163 | POLYCAST INC | 14140 SW 72ND AVE<br>SUITE 100 | TIGARD, OR 97224 |
| TK2058 | TDK CORPORATION OF AMERICA | 1600 FEEHANVILLE DRIVE | MOUNT PROSPECT, IL 60056 |
| TK2548 | XEROX CORPORATION | 14181 SW MILLIKAN WAY | BEAVERTON, OR 97005 |
| TK2565 | VISION PLASTICS INC | 26000 SW PARKWAY CENTER DRIVE | WILSONVILLE, OR 97070 |
| TK6314 | MCX INC | 1315 OREGON AVE | KLAMATH FALLS, OR 97601-6540 |

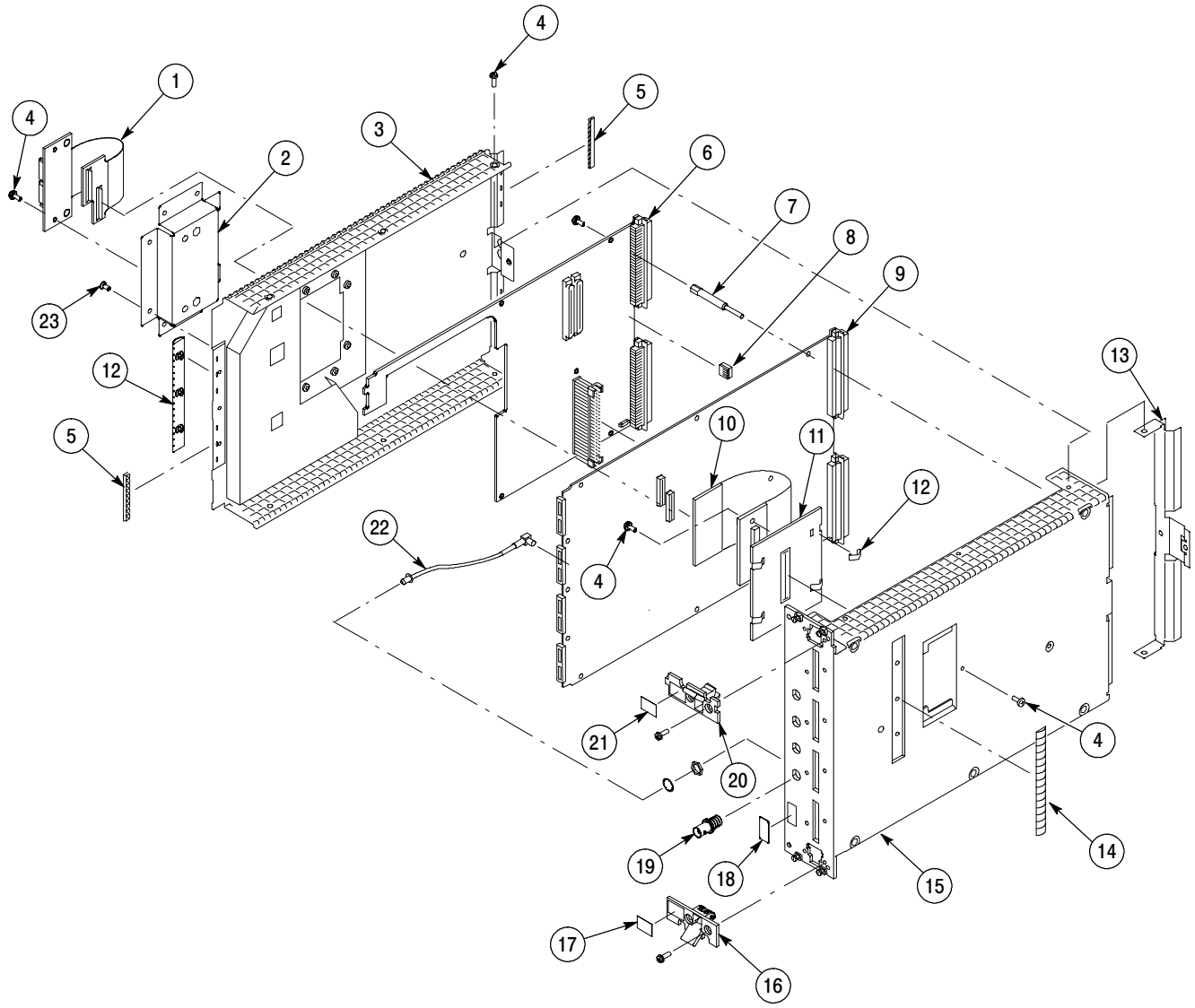


**Figure 10-1: TLA7AAX and TLA7ABX Logic Analyzer Module exploded view**

## Replaceable parts list

| Fig. & index number | Tektronix part number | Serial no. effective | Serial no. discont'd | Qty | Name & description | Mfr. code | Mfr. part number |
|---|---|---|---|---|---|---|---|
| 10-1-1 | 671-5339-00 | | | 1 | CIRCUIT BD ASSY:MERGE CONNECTOR,LEFT SIDE, TESTED, TLA7AA3, TLA7AA4, TLA7AB4 | 80009 | 671-5339-00 |
| -2 | 407-4859-00 | | | 1 | BRACKET:MERGE,COVER,LEFT SIDE,0.050 AL, TLA7AA3, TLA7AA4, TLA7AB4 | TK1943 | 407-4859-00 |
| | 407-4860-00 | | | 1 | BRACKET:BLANK FLAT,MERGE,COVER,LEFT SIDE,0.050 AL, TLA7AA1, TLA7AA2, TLA7AB2 (NOT SHOWN) | TK1943 | 407-4860-00 |
| -3 | 200-4672-00 | | | 1 | COVER:TWO WIDE,0.062 AL,TLA700 SERIES, | TK1943 | 200-4672-00 |
| -4 | 211-0409-00 | | | 22 | SCR,ASSEM WSHR:4-40 X 0.312,PNH,STL,CDPL,T-10 TORX DR | 0KB01 | 211-0409-00 |
| -5 | 348-1537-00 | | | 6 | GASKET,EMI:CLIP-ON,1.98 L,BE CU,TIN PLATED,W/T LANCES | 0KM03 | 0493011500 |
| -6 | 671-5312-00 | | | 1 | CIRCUIT BD ASSY:LPU, LOCAL PROCESSOR UNIT | 80009 | 671-5312-00 |
| | 150-1278-00 | | | 3 | DIODE,OPTO:LED,GRN,569NM,2MCD AT 5V,60 DEG VIEW ANGLE,INTEGRAL RES,TINTED, DIFFUSED, RIGHT AN (NOT SHOWN) | 83330 | 551-0607 |
| | 150-1279-00 | | | 1 | DIODE,OPTO:LED,YELLOW,585NM,2MCD AT 5V,60 DEG VIEW ANGLE,INTEGRAL RES,TINTED DIFFUSED,RIGHT (NOT SHOWN) | 0MS63 | MR5360 MP4B |
| -7 | 129-1478-00 | | | 5 | SPACER, POST:1.738 L,1.113 SPACING,W/ 0.35 L,0.25 HEX,W/ 4-40 INT THD X 6-32 EXTERNAL THD,NIC | TK0588 | 129-1478-00 |
| -8 | 260-2597-00 | | | 2 | SWITCH,ROTARY:HEXADECIMAL,100MA AT 50VDC,RIGHT ANGLE,0.430 W X 0.400 H X 0.202 L | 81073 | 94HAB16RA |
| -9 | 671-5351-00 | | | 1 | CIRCUIT BD ASSY:34 CH,64MB, DDR, ACQUISITION, TLA7AA1 | 80009 | 671-5351-00 |
| | 671-5350-00 | | | 1 | CIRCUIT BD ASSY:68 CH,64MB, DDR, ACQUISITION, TLA7AA2 | 80009 | 671-5350-00 |
| | 671-5349-00 | | | 1 | CIRCUIT BD ASSY:102 CH,64MB, DDR, ACQUISITION, TLA7AA3 | 80009 | 671-5349-00 |
| | 671-5311-00 | | | 1 | CIRCUIT BD ASSY:136 CH,64MB, DDR, ACQUISITION, TLA7AA4 | 80009 | 671-5311-00 |
| | 671-5441-00 | | | 1 | CIRCUIT BD ASSY:68 CH,256MB, DDR, ACQUISITION, TLA7AB2 | 80009 | 671-5441-00 |
| | 671-5442-00 | | | 1 | CIRCUIT BD ASSY:136 CH,256MB, DDR, ACQUISITION, TLA7AB4 | 80009 | 671-5442-00 |
| -10 | 671-5340-00 | | | 1 | CIRCUIT BD ASSY:MERGE CONNECTOR,RIGHT SIDE,TESTED, TLA7AA3, TLA7AA4, TLA7AB4 | 80009 | 671-5340-00 |
| -11 | 407-4861-00 | | | 1 | BRACKET:MERGE,CHASSIS,RIGHT SIDE,0.062 AL, TLA7AA3, TLA7AA4, TLA7AB4 | TK1943 | 407-4861-00 |
| | 407-4862-00 | | | 1 | BRACKET:BLANK FLAT,MERGE,CHASSIS,RIGHT SIDE,0.062 AL, TLA7AA1, TLA7AA2, TLA7AB2 (NOT SHOWN) | TK1943 | 407-4862-00 |
| -12 | 131-6643-00 | | | 4 | CONTACT,ELEC:GROUNDING,0.169 L,0.320 DEEP,ELECTROLESS NICKEL,TDS3012 | 0KM03 | 131-6643-00 |

## Replaceable parts list (cont.)

| Fig. & index number | Tektronix part number | Serial no. effective | Serial no. discont'd | Qty | Name & description | Mfr. code | Mfr. part number |
|---|---|---|---|---|---|---|---|
| 10-1-13 | 386-6868-00 | | | 1 | PANEL,VXI:VXI APPLICATION,TWO-WIDE,VENUS 2,BACK PANEL,SAFETY CONTROLLED | TK1943 | 386-6868-00 |
| -14 | 348-1365-01 | | | 2 | SHLD GSKT,ELEC:SYMETRICAL SLOTTED FINGER,0.350 W X 7.5 L,RIVIT MTG,SNAP-IN,RIVIT SPACING 1.5 IN | 0KM03 | 0493-0070-00 |
| -15 | 441-2257-00 | | | 1 | CHASSIS ASSY:34 CH,W/SUB FRONT PANEL & LEXAN,0.62 AL,TLA7AA1 | TK1943 | 441-2257-00 |
| -15 | 441-2258-00 | | | 1 | CHASSIS ASSY:68 CH,W/SUB FRONT PANEL & LEXAN,0.62 AL,TLA7AA2, TLA7AB2 | TK1943 | 441-2258-00 |
| -15 | 441-2259-00 | | | 1 | CHASSIS ASSY:102 CH,W/SUB FRONT PANEL & LEXAN,0.62 AL,TLA7AA3 | TK1943 | 441-2259-00 |
| -15 | 441-2260-00 | | | 1 | CHASSIS ASSY:136 CH,W/SUB FRONT PANEL & LEXAN,0.62 AL,TLA7AA4, TLA7AB4 | TK1943 | 441-2260-00 |
| -16 | 367-0484-00 | | | 1 | HANDLE,EJECTOR:INJECTOR/EJECTOR ASSEMBLY,TWO WIDE VXI,W/OUT KEYING,SPRING LOADED,PLASTIC,20% GL | 7X318 | 1462 |
| -17 | 335-0646-00 | | | 1 | MARKER,IDENT:LABEL,MKD FOR USE WITH TLA700 SERIES,BOTTOM INJECTOR/EJECTOR,0.745 X 0.520,0.010 | 0KB05 | 335-0646-00 |
| -18 | 335-0639-00 | | | 1 | MARKER,IDENT:CONFIGURATION LABEL,MKD TIMING,STATE SPEED,RAM DEPTH,0.475 X 0.975,0.010 POLY,GE | 0KB05 | 335-0639-00 |
| -19 | 131-1315-01 | | | 4 | CONN,RF JACK:BNC,PNL,50 OHM,FEMALE,STR,PELTOLA/PNL MNT,SILVER ALLOY,0.576 MLG X 0.366 TERMN, | 24931 | 28JR306-1 |
| -20 | 367-0483-00 | | | 1 | HANDLE:INJECTOR/EJECTOR ASSEMBLY,TWO WIDE VXI,W/KEYING,SPRING LOADED,PLASTIC,20% GLASS- | 7X318 | 2TEK 1461 |
| -21 | 335-0640-00 | | | 1 | MARKER,IDENT:LABEL,MKD TLA7AA1, 34CH,TOP INJECTOR/EJECTOR,0.745 X 0.520,0.010 POLY,GE LEXAN,W/ADHE | 0KB05 | 335-0640-00 |
| | 335-0641-00 | | | 1 | MARKER,IDENT:LABEL,MKD TLA7AA2, 66CH,TOP INJECTOR/EJECTOR,0.745 X 0.520,0.010 POLY,GE LEXAN,W/ADHE | 0KB05 | 335-0641-00 |
| | 335-0642-00 | | | 1 | MARKER,IDENT:LABEL,MKD TLA7AA3, 102CH,TOP INJECTOR/EJECTOR,0.745 X 0.520,0.010 POLY,GE LEXAN,W/ADHE | 0KB05 | 335-0642-00 |
| | 335-0643-00 | | | 1 | MARKER,IDENT:LABEL,MKD TLA7AA4, 136CH,TOP INJECTOR/EJECTOR,0.745 X 0.520,0.010 POLY,GE LEXAN,W/ADHE | 0KB05 | 335-0643-00 |
| | 335-0644-00 | | | 1 | MARKER,IDENT:LABEL,MKD TLA7AB2, 68CH,TOP INJECTOR/EJECTOR,0.745 X 0.520,0.010 POLY,GE LEXAN,W/ADHE | 0KB05 | 335-0644-00 |
| | 335-0645-00 | | | 1 | MARKER,IDENT:LABEL,MKD TLA7AB4, 136CH,TOP INJECTOR/EJECTOR,0.745 X 0.520,0.010 POLY,GE LEXAN,W/ADHE | 0KB05 | 335-0645-00 |
| -22 | 174-4542-00 | | | 4 | CA ASSY,RF:COAXIAL,50 OHM,8.0 L,MCX TO PELTOLA | 060D9 | 174-4542-00 |

## Replaceable parts list (cont.)

| Fig. & index number | Tektronix part number | Serial no. effective | Serial no. discont'd | Qty | Name & description | Mfr. code | Mfr. part number |
|---|---|---|---|---|---|---|---|
| -23 | 211-0486-00 | | | 8 | SCREW,MACHINE:4-40 X 0.168 L,FLH,100 DEG,TORX T-9 | 0KB01 | 211-0486-00 |
| | 174-4595-00 | | | 4 | CABLE ASSY:BNC - BNC,10X ATTENUATION,50 OHM COAX | 060D9 | 174-4595-00 |
| | 071-0863-02 | | | 1 | MANUAL,TECH:USER,V4.1 SOFTWARE,TLA SERIES,DP | TK2548 | 071-0863-02 |
| | | | | | **Optional Accessories** | | |
| | 071-1043-00 | | | 1 | MANUAL,TECH:SERVICE, LOGIC ANALYZER MODULES,TLA700 SERIES,DP | TK2548 | 071-1043-00 |
| | 071-0912-00 | | | 1 | MANUAL,TECH:EXPANSION MAIN FRAME SERVICE,TLA7XM,TLA721 | TK2548 | 071-0912-00 |
| | 071-0913-00 | | | 1 | MANUAL,TECH:MAIN FRAME SERVICE,TLA715,DP | TK2548 | 071-0913-00 |
| | 071-0865-02 | | | 1 | MANUAL,TECH:INSTRUCTION,TLA700 SERIES MAINFRAME FIELD UPDRADE,TLA7UP,DP | TK2548 | 071-0865-02 |
| | 071-0866-02 | | | 1 | MANUAL,TECH:INSTRUCTION,TLA600 SERIES MAINFRAME FIELD UPDRADE,TLA6UP,DP | TK2548 | 071-0866-02 |
| | 071-1059-00 | | | 1 | MANUAL,TECH:INSTRUCTION,P6810,P6860,P6880 LOGIC ANALYZER PROBES,DP | TK2548 | 071-1059-00 |
| | 070-9793-02 | | | 1 | MANUAL,TECH:MASS,TERMINATION PROBE,P6434 | TK2548 | 070-9793-02 |
| | 020-2451-00 | | | 1 | ACCESSORY KIT:ELASTOMER HOLDER ASSEMBLIES,BAG OF (2) 352-1092-00,THIN BOARD | TK1163 | 020-2451-00 |
| | 020-2452-00 | | | 4 | ACCESSORY KIT:ELASTOMER HOLDER ASSEMBLIES,BAG OF (2) 352-1093-00,THICK BOARD | TK1163 | 020-2452-00 |
| | 020-2453-00 | | | 1 | ACCESSORY KIT:NUTBLOCK ASSEMBLIES,BAG OF (2) 220-0255-00 | TK1163 | 020-2453-00 |
| | 020-2455-00 | | | 1 | ACCESSORY KIT:COMPRESSION-ON-PCB TO MICTOR ADAPTER,17 CH,BAG INCLUDES 671-5528-00,ELASTOMERS H | 80009 | 020-2455-00 |
| | 020-2456-00 | | | 1 | ACCESSORY KIT:COMPRESSION ON PCB TO MICTOR ADAPTER,34 CH,BAG INCLUDES 671-5449-00,ELASTOMER HO | 80009 | 020-2456-00 |
| | 020-2457-00 | | | 1 | ACCESSORY KIT:MICTOR-ON-PCB TO COMPRESSION ADAPTER,INCLUDES 671-5294-00 | 80009 | 020-2457-00 |

## Replaceable parts list

| Fig. & index number | Tektronix part number | Serial no. effective | Serial no. discont'd | Qty | Name & description | Mfr. code | Mfr. part number |
|---|---|---|---|---|---|---|---|
| | | | | | **TLACAL2 Standard Accessories** | | |
| | 174-4138-00 | | | 8 | CABLE ASSY,RF:COAXIAL,50 OHM,OPTICAL BD TO ACQ BD | 060D9 | 174-4138-00 |
| | 174-4678-00 | | | 4 | CA ASSY,SP:RIBBON,28 AWG,24.0 L,IDC,FEMALE,2 X 17,0.100 CTR,PLZ,DUAL ENDED,MIC/PIC TO MAIN | 060D9 | 174-4678-00 |
| | 161-0104-00 | | | 1 | Cable Assembly:3,18 AWG, 98 L, 125V/10Amp, Right Angle, IEC320, NEMA 15-5P, with Cord Grip, US, | S3109 | ORDER BY DESCRIPTION |
| | 012-1379-00 | | | 1 | Cable Assembly:RS232, 76.0 L ,9, 24 AWG DB9 Female X DB9 Female, Serial Null Modem | TK6314 | 012-1379-00 |
| | 650-4298-00 | | | 4 | MIC BOARD ASSY:MODULE INTERFACE CARD,W/COVERS | 80009 | 650-4298-00 |
| | 650-4299-00 | | | 1 | PIC BOARD ASSY:PROBE INTERFACE CARD,W/COVERS | 80009 | 650-4299-00 |
| | 016-1315-00 | | | 1 | MARKER BAND SET:For Probe Identification,2 Each of 5 Colors | 7X318 | 1134 |
| | P6041 | | | 4 | BNC-TO-SMB cable | 80009 | P6041 |
| | 071-1125-00 | | | 1 | TLACAL2 Instruction Sheet | TK2548 | 071-1125-00 |
| | 159-0356-00 | | | 1 | FUSE,CARTRIDGE:5.0MM X 20MM,1.0A,250V HIGH BREAKING CAPACITY,UL,SEMKO, INSTALLED | 71400 | GDA-1 |
| | 159-0351-00 | | | 1 | FUSE,CARTRIDGE:5 X 20MM,0.5A,250,HIGH BREAKING CAPACITY,CERAMIC,UL REC,VDE,SEMKO | 61935 | 001.1001 |
| | 012-0991-00 | | | 1 | CABLE, INTERCON:GPIB, COMPOSITE SHIELDING | 00779 | 553577-3 |
| | 174-4138-00 | | | 8 | CABLE ASSY,RF:COAXIAL,50 OHM,OPTICAL BD TO ACQ BD | 060D9 | 174-4138-00 |